FLARES: Flexible Architecture for Embedded Systems

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Main Objectives

- Study the compilation requirements for reconfigurable computing
- Explore the adaptive EPIC processor space
  - Static architectural space exploration
  - Dynamically reconfigurable processors
The Framework

User Application → Profiling

Compiler --> Architectural Space Explorer

Compiled Code → Co-simulator

Synthesis Tools

User Requirements

Arch. Library
Adaptive EPIC processing

Partitioning of code into hardware and software component via the compiler and profiling

- Automatic generation of hardware via Handel-C
- Automatic generation of interface
The Baseline AEPIC
Work in Progress

Convert from Rebel to Handel-C

Output FPGA Bit File

Select Hotspots

Extensions to Simulate AEPIC

Interface with FPGA
Achievements to Date (1)

- Automatic generation of synthesizable Handel-C code from Trimaran’s Rebel compiler intermediate language

- Experiments with optimum structures for HDL synthesis
Achievements to Date (2)

- Simulation of full Adaptive EPIC instruction set
- Remote connection to place-and-route server to obtain realistic estimates
### Benchmark Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>EPIC cycles</th>
<th>AEPIC cycles</th>
<th>FPGA cycles</th>
<th>FPGA freq.</th>
<th>AEPIC Speedup</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADPCM Dec</td>
<td>5708383</td>
<td>2266857</td>
<td>411280</td>
<td>20MHz</td>
<td>2.52</td>
</tr>
<tr>
<td>G721 Enc (optimized/1CFU)</td>
<td>62002864</td>
<td>49730341</td>
<td>402884</td>
<td>60MHz</td>
<td>1.25</td>
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<td>G721 Enc (2 CFUs)</td>
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<td>G721 Dec (2 CFUs)</td>
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<td>8528970</td>
<td>20MHz</td>
<td>2.64</td>
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</tbody>
</table>

**Performance on AEPIC**

- ADPCM Dec
- G721 Enc (optimized/1CFU)
- G721 Dec (optimized/1CFU)
- G721 Enc (2 CFUs)
- G721 Dec (2 CFUs)
## Automatic Hardware Generation Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Our Approach</th>
<th>Straight Hand code (no par/optimization)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Clock Cycles</td>
<td>Clock Length (ns)</td>
</tr>
<tr>
<td>Fir2dim (DSPStone)</td>
<td>557</td>
<td>20.076</td>
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<tr>
<td>Iir (DSPStone)</td>
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<tr>
<td>N complex update (DSPStone)</td>
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<td>87.365</td>
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<td>Matmul</td>
<td>501</td>
<td>131.88</td>
</tr>
</tbody>
</table>
Progress to Date

User Application → Profiling

Compiler → Compiled Code

Architectural Space Explorer

User Requirements

Arch. Library

Synthesis Tools

Co-simulator
Looking for collaborators

- Models for physical designs
  - Estimates of gate count and cycle length from intermediate code

- Synthesis backends
  - VHDL or Verilog
  - Beyond FPGAs: Triscend and other chips
  - Soft-cores
谢谢！