Unified Quadratic Programming Approach For 3-D Mixed Mode Placement

Haixia yan, Zhuoyuan Li, Qiang Zhou, Xianlong Hong

EDA LAB, Tsinghua University, Beijing China
Outline

- Background
  - 3-D placement algorithm
    - Global Placement
    - Layer Assignment
    - Detailed Placement
  - Results
- Conclusions
Background

➢ Development of VLSI

  Character size

  Power supply

  The number of transistors

➢ Effort in the future

  Increase transistor device capabilities

  Improve the performance of the wires
Background

How to reduce the interconnect delay?
Background

- **Advantages**
  1. Chip Area
  2. Integration
  3. Interconnect Delay

- **challenges**
  1. Complexity of design
  2. Heat dissipation
  3. Cost of design
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3-D Placement Algorithm

Objective

- Distribute the cells into the different layers with no overlaps
- Subject to area, wire length or other performance

Placement methods

- Force-directed method
- Quadratic programming method
- Hierarchical method
- ……
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Global Placement

➢ Task

-- Distribute the cells in the 3D space to get the optimum position with overlap allowed and to meet some performance requirement such as wire length, delay or congestion.

➢ Assumptions

-- The 3D space is a cube with the height $H$ of it defined by the user

-- Cells have the same height $h$

$$h = \frac{H}{N_{\text{layer}}}$$
Global Placement

- **Objective Function**

\[ OBJ = WL + \beta \cdot DIST \]

- **WL - Wire Length**

\[ WL = \sum_{\text{forall nets } ij} w_{ij} \{(x_i - x_j)^2 + (y_i - y_j)^2 + (z_i - z_j)^2\} \]

Net \( n_{ij} \) is a two pin net, connecting the cell \( i \) and cell \( j \).

\( w_{ij} \) is the weight of Net \( n_{ij} \)
Global Placement

➢ DIST - Distribution Cost

Bin Density:

\[ D_{ijk} = \frac{\text{cellvolume}_{ijk}}{\text{binvolume}_{ijk}} \]

Discrete cosine Transformation (DCT):

\[ F = DCT(D) = \{f_{ijk}\} \]

\[ f_{ijk} = \sqrt{\frac{8}{N^2M}} C(i)C(j)C(k) \sum_{x=0}^{N-1} \sum_{y=0}^{N-1} \sum_{z=0}^{M-1} d_{xyz} \cos \left( \frac{(2x+1)ip}{2N} \right) \cos \left( \frac{(2y+1)jp}{2N} \right) \cos \left( \frac{(2z+1)kp}{2M} \right) \]

Distribution Cost:

\[ DIST = \sum_{i,j,k} u_{ijk} f_{ijk}^2 \]

\[ u_{ijk} = \frac{1}{(i+j+k+1)} \]
Global Placement

DCT – Discrete Cosine Transformation

Reflect the distribution more accurately!

DIST = 4.08  DIST = 3.46  DIST = 3.16
Global Placement

- Unify the wire length object and distribution cost into a quadratic function

\[ \text{DIST} = \frac{1}{2} a_i x_i^2 + b_i x_i + c_i \]

\[ (x_i - \delta, \text{DIST}_1, (x_i, \text{DIST}), (x_i + \delta, \text{DIST}_2) \]
Global Placement

3-D Global Placement Flow

- Initial Solution
- Spread Cells and Compute DIST
- Update Coefficient and Solve Equation
- Solution Optimization

The Successive Over Relaxation (SOR) method
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Layer assignment

➢ Task

-- Assign the cells into different layers

➢ Constraints

-- chip area
-- wire length
-- number of vertical vias
-- other performance
Layer Assignment

- Even chip area

Z – Direction

- The number of vertical vias
- Bin density of every layer

\[ \text{Cost} = \text{ViaInc} + b \times \sum_{\text{BinsIncludeCelli}} \max(0, (\text{BinDensity} - 1)) \]
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Detailed Placement

➢ Task

--Remove overlaps in every layer and optimize chip performance

➢ Flow

- Net Decomposition
- Detailed Placement On Each Layer
- K times iteration
Detailed Placement

- Net Decomposition
- Detailed placement in every layer – resolve the overlap and optimize the wire length [1]

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Results

>Benchmark

<table>
<thead>
<tr>
<th>Benchmark</th>
<th># Nets</th>
<th># Cells</th>
<th># Macro</th>
<th># Pads</th>
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--Mixed-mode :standard cells and macro blocks.

-- Pads are fixed around the lowest layer of the chip.
Results

- Compared with 2D (1 layers) placement on wire length
  - 2 layers: wire length 12%-16% reduction
  - 3 layers: wire length 19%-26% reduction
  - 4 layers: wire length 23%-32% reduction

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<th>1 Die WL</th>
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Conclusions

- **Discrete cosine transformation**
  
  Help to finish the distribution of cells

- **Layer assignment algorithm**
  
  Considering the layer assignment during the global placement, not after placement.

- **Improve the performance of the placement algorithm**
  
  Optimize the congestion, delay or other objective.
Thank You!

Contact Info:
Haixia Yan
yhx03@mails.tsinghua.edu.cn