The SuperK Project at MPRC

Xianfeng LI (李险峰)

Microprocessor Research and Development Center (MPRC)
Peking University
What Is SuperK

- **A project on low-cost, portable computers**
  - UniCore architecture
  - Hardware multimedia enhancement
  - Flash disk
  - Single-chip solution

- **Two product lines**

OLPC-like: ~1000RMB

UMPC-like: 3C computer
SuperK SoC Architecture

Globally-Asynchronous-Locally-Synchronous (GALS)
UniCore II Overview

- **TSMC 0.13um**
  - Clock rate: 600 MHz

- **TSMC 90nm**
  - Clock rate: 800 MHz
### Int/ FP Units

- **UniCore32**
  - 8-stage pipeline
  - 7 operation modes
  - Dynamic branch prediction
  - Precise interrupt

- **UniCore-F64**
  - IEEE-754 standard
  - 2D/3D ISA extensions
  - Floating-point Register file
    (32 x 32-bit or 16 x 64-bit)
  - Precise interrupt
Other Core Components

- **Coprocesors**
  - CP0, OCD

- **Caches**
  - Decoupled I/D caches
  - 16KB, 4-way

- **MMUs**
  - Hierarchical TLBs
  - Support multiple page sizes

- **Dual-port BIU**
  - 64-bit memory access bus
  - 32-bit high-speed system bus
UniGFX Graphics Engine

- Efficient HW implementation of 2D graphics operations (Line Draw/ROP/BLT/Alpha Blending/…)
- GUI acceleration
UniGFX Video Engine

- HW/SW co-operated video decoding
  - UniCore: Predecoding
  - MME: IDCT, MC

- Dedicated HW for H.264 codec
  (collaboration with Prof. Y-L Lin’s group, TW NTHU)
UniGFX Display Engine

- Supports GFX and Video display channel
- Supports HW Cursor
- Supports VGA interface
- Inner DMA channels for display data fetching
## Pressures on Bus and Memory

<table>
<thead>
<tr>
<th>Module</th>
<th>Bandwidth (MB/s)</th>
<th>Characters</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Behavior</td>
<td>Real Time Req.</td>
</tr>
<tr>
<td>DE</td>
<td>180</td>
<td>Constant</td>
<td>Hard</td>
</tr>
<tr>
<td>VE</td>
<td>≤60</td>
<td>Varies with stream</td>
<td>High</td>
</tr>
<tr>
<td>GE</td>
<td>~20</td>
<td>Random &amp; Bursty</td>
<td>High</td>
</tr>
</tbody>
</table>

### Real Time Req. Behavior Condition

**Bandwidth (MB/s)**

- **Module**
  - DE
  - VE
  - GE

**Characters**

- **Behavior**
  - Constant
  - Varies with stream
  - Random & Bursty

**Real Time Req.**

- Hard
- High

**Condition**

- 1024X768 @60fps, 32bpp
- 720X576@25fps, YUV420
- 1024X768 @32bpp
Demo - H.264
Bus Structure

- Graphics & Multimedia Devices
- Dual-Port UniCore-2 CPU
  - 64-bit AHB, High Clock Freq
  - Arbiter & Monitor
  - Dual-Port DDR-II SDRAM Controller
- Low-Speed Peripheral Devices
  - 32-bit APB, Low Clock Freq
  - Arbiter & Monitor
  - APB Bridge
  - High-Speed Peripheral Devices
- 32-bit AHB, Medium Clock Freq
Bus Monitor

Bus Signals Probe

- HCLK
- HTRANS
- HADDR
- HREADY
- HWRITE

Multi-Mode Bus Monitor

Bus Master Behavior Recorder

Bus Idle  Start  Wait Data  Transfer Data  Bus Idle

Master 1
Transfer Data
32934 Cycles

Bus Idle
9094 Cycles

Bus Occupancy Summary

Master 2
Wait Data
7375 Cycles

Master 3
Wait Grant
17342 Cycles
Verification

Simulation
(test vectors, small programs)

FPGA
(real-life programs, OS)
SURP: A Verification Platform

- **SURP = Scalable, Unified, Reusable Platform**
  - Implementation: OpenVera + Synopsys RVM library
  - Can generate different kinds of stimuli at any of the five layers
  - Functional coverage monitoring
Benefits

- Multiple IPs were verified with SURP
  - 3x verification efficiency

- Amount of testing code: 70% reduction

- Found a bug in bus arbiter

- Clock-Domain-Crossing (CDC) faults [DATE’07]
FPGA Verification

- **Dual-chip solution**
  - Two Xilinx XC4VLX200 chips, connected via LVDS
  - DDR/DDR2 SDRAM slots
  - Two NAND flash chips
  - On-board VGA/USB/MAC PHYs
  - PCI, IDE slots
  - JTAG
Transaction Level Model (TLM) - The First Cut
# Performance Validation

<table>
<thead>
<tr>
<th></th>
<th>bit rate</th>
<th>decode speed (fps)</th>
<th>difference</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>TLM</td>
<td>FPGA</td>
</tr>
<tr>
<td>mpeg2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4300K</td>
<td>4.92</td>
<td>4.49</td>
</tr>
<tr>
<td></td>
<td>6000K</td>
<td>4.11</td>
<td>4.02</td>
</tr>
<tr>
<td></td>
<td>8000K</td>
<td>3.61</td>
<td>3.66</td>
</tr>
<tr>
<td></td>
<td>10000K</td>
<td>3.21</td>
<td>3.33</td>
</tr>
<tr>
<td></td>
<td>12000K</td>
<td>2.91</td>
<td>3.04</td>
</tr>
<tr>
<td>mpeg4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2600K</td>
<td>3.38</td>
<td>3.56</td>
</tr>
<tr>
<td></td>
<td>4000K</td>
<td>2.97</td>
<td>3.09</td>
</tr>
<tr>
<td></td>
<td>6000K</td>
<td>2.63</td>
<td>2.71</td>
</tr>
<tr>
<td></td>
<td>8000K</td>
<td>2.36</td>
<td>2.30</td>
</tr>
<tr>
<td></td>
<td>10000K</td>
<td>2.14</td>
<td>2.15</td>
</tr>
<tr>
<td></td>
<td>12000K</td>
<td>1.98</td>
<td>2.00</td>
</tr>
</tbody>
</table>
Evaluation Results

- **MPEG2-Decide Rate**
  - Graph showing decode rate in fps across different bps (4300K to 12000K).
  - Peak rate at 4300K bps.

- **MPEG2-UniCore Memory Accesses**
  - Graph showing memory accesses in MBytes across different bps (4300K to 12000K).
  - Blue line for read accesses, pink line for write accesses.

- **MPEG2-High-speed Bus Usage**
  - Graph showing bus usage percentage across different bps (4300K to 12000K).
  - Uptrend of usage from 3.55% at 4300K to 3.80% at 12000K.

- **MPEG2-MME Memory Access**
  - Graph showing memory access in MBytes across different bps (4300K to 12000K).
  - Blue line for read accesses, pink line for write accesses.
Future work

Model construction (UniCore + MME) →
Model validation (UniCore + MME) →
Performance evaluation (UniCore + MME) →
Model construction (full-fledged) →
Model optimization (performance-accuracy tradeoff)

Performance evaluation/Design space exploration →
Issues

- Timing
- Power
- DFT
- DFM
- Packaging
Timing Improving Techniques

- **Challenges**
  - Core: TSMC 0.13um, 600 MHz – tough job for standard cell-based design
  - Die size: 7x7
  - Pin number: 750
  - 8 clock domains

- **Useful skew**
  - Traditional clock skew scheduling (CSS): 6.4%
  - Our algorithm: 26% [DAC’06]

- **Other tricks**
  - ~10% additional improvement...
Power Considerations

- **Dynamic Power**
  - Clock gating: \(~30\%\) reduction

- **Static Power**
  - Multi-VT technique: high-Vt cells for non-critical paths
  - EDA tools: \(~20\%\) reduction
  - Our replacement algorithm: \(~20\%\) more reduction
Test data compression

- Test data: 431M (after dynamic compaction)
- Mentor: 10x compression
- Our algorithm: 43x compression

[ICCAD’07]
- Dummy metal insertion and double via for higher product yield
- Fix SI violations caused by dummy metal
- Several iterations between timing optimization and DFM
Packaging - Flipchip

■ Motivation
  □ IR drop problem
  □ Thermal consideration
  □ Electrical consideration

■ Approach
  □ Peripheral IO design
  □ Using Cu for RDL
  □ Bump template for self-adjustment
Software System

- Application System
- Linux Kernel
- Device Drivers
- Bootloader
- glibc
- ld
- gcc
- as

SuperK SoC
Software Development Platforms

- **System-level simulator**
  - Linux kernel porting

- **FPGA Board**
  - Verification of SoC modules
  - Driver development

- **ASIC board**
  - Software integration
  - Linux kernel porting
Toolchain

- **Porting to UniCore architecture**
  - gcc, ld, as, glibc

- **Integrated Development Environment (IDE)**
  - Based on Eclipse
  - Native execution or simulation

- **Debugging**
  - Remote GDB

- **Optimizations**
  - Link-time optimization
  - Code compaction
  - memory access reductions
Applications

• Graphics support
  • X-window
  • Gnome

• Key applications
  • Openoffice
  • Mozilla Firefox, email client, multimedia player
  • JVM

• Software package management tool

• Chinese language support
Summary

- **A Single-chip solution**
  - UniCore based
  - SoC-centric
  - Hardware multimedia enhancement

- **Project progress**
  - Multi-disciplinary work
  - Close collaboration of ~8 teams
  - First chip: late this year