Integration and Automation
KEY to Productivity Boost in Analog and Mixed Signal Designs

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Magma Design Automation, Inc.
World is Mixed Signal...And Integrated

Talk  Listen  Watch

Capture

Create
Mixed Signal = Digital + Analog/Custom

The International Technology Roadmap for Semiconductors (ITRS)

The cutting edge of DIGITAL design is 45nm. Active tape outs have been done.

The bleeding edge of ANALOG design is 90nm, and many are trapped at 130 and 250nm (5 to 10 year old technology!)
Outline

• The Evolution of Digital Tools
• The Evolution of Analog Tools
• The Requirements for Analog Automation
• Mixed Signal Considerations
• Magma 2.0 – Titan
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Evolution of Digital Tools

- **1960s**
  - Capture design by hand crafting
  - Functional and timing verification by visual inspection
  - Implementation by hand drawing

- **1970s**
  - Capture design by gate level schematics
  - Functional verification through event driven logic simulation
  - Timing verification by STA

- **1980s**
  - Capture design by RTL
  - Automated logic synthesis
  - Automated place and route
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1970s
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- Functional verification through event driven logic simulation
- Timing verification by STA
- Analog simulation via SPICE

1990s
- Capture design by RTL
- Automated logic synthesis
- Automated place and route
- Capture design by transistor level schematics
Limitation of Today’s Analog Tools

- Most of today's analog tools were conceived in 1990s
  - The underlying architectures were never intended to support the sophisticated demands of a mixed-signal design environment
- Today's analog design and verification tools are essentially limited to transistor-level schematics
- Very limited success w.r.t. automation
  - Representing analog functionality at a high-level of abstraction and then using these representations to generate transistor-level equivalents
  - Automatically optimizing analog circuits
  - Automatically placing-and-routing analog circuits
Digital Design is Automated, Reusable

Digital

Synthesis, Place & Route
Turnaround Time
2 Days

Digital Logic
- Custom Digital Cells
- ADC
- SERDES
- PLL
- Memory

Digital is Automated, Reusable
Analog / Custom Design is NOT Automated, NOT Reusable

Digital

Integration
Turnaround Time
4-8 Weeks

Synthesis, Place & Route
Turnaround Time
2 Days

Analog

IP Process Migration
Turnaround Time
6-12 Months

Transcievers, SERDES...
Turnaround Time
3-6 Months
Why?

For every new process node, designs have to be re-created by-hand from scratch.

It’s a Very Hard Problem To Solve!
Mixed Signal = Digital + Analog/Custom

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Wish List for Next Generation Analog Tools

• The ability to specify an analog function at a high level of abstraction and to then automatically translate this representation into its transistor-level equivalent
• The ability to automatically perform analog refinement and optimization
• The ability to automatically place analog components on the IC
• The ability to automatically route analog components on the IC
• The capability to automate the migration process for an analog design from one process/technology node to another and from one foundry to another
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Wish List for Next Generation Mixed Signal Tools

- Analog and digital design and verification engines should employ a unified database
- The environment must provide extreme capacity and performance
  - Such as loading the entire full-chip database in a minute or less and re-drawing all of the analog and digital layers in seconds
- The environment must support extremely accurate parasitic extraction and full-chip mixed-signal simulation and analysis
- At the chip-finishing stage, the environment must support automatic global routing
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# Magma 2.0: Mixed-Signal Design

## Analog IP Process Migration *

## Integrated Simulation Environment Including Waveform Editor

## Schematic Editor

## Layout Editor

## Shape Based, Constraint Driven Routing

## Mixed Signal Physical Constraints *

## Digital & Analog Integration

## Integrated Full Chip LVS, DRC and Extraction

## Full Chip Timing / Signal Noise Analysis

## United Custom And Digital Database

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**Titan: Mixed-Signal Platform**

* Beta / Limited production now Full Production Q3-08
Driving the Shift to **Titan**

- **Accuracy**
  - Production proven FineSim integrated simulation environment

- **Automation**
  - Analog IP process migration automation

- **Integration → Ease of Use**
  - Integration to support digital, custom, analog flows seamlessly
    - Integration with FineSim, Talus, Quartz DRC/LVS

- **Faster time to tapeout**
  - Up to 10x speed and capacity advantage over old solutions
  - Speed and capacity to iterate quickly and close

- **Smooth Migration Path**
  - OpenAccess Compatibility
  - Easily transition existing design to Titan
Titan: The Only Mixed-Signal Platform

Embedded Talus
Titan: High Speed, High Capacity Layout & Schematic Editor

- Responsive all-layer redraw, pan & zoom
- Integrated GUI with menus, hotkeys & tear-off panels
- Fully scriptable Tcl/Tk interface
- Cell hierarchy browser
- Edit-in-place correct across hierarchy
- Full cross-probing: schematics, DRC errors & parasitics

Example: Layout Editing of 42GB GDSII Design

- Full Chip Open → 4 min
- Redraw → 8 sec
- Zoom In by 2 → 4 sec
- Pan time to random points → 7 sec
Titan Accuracy

**FineSim SPICE : Fastest Spice Simulator**

- Unified Single Executable Simulator
  - Native-Parallel™ Technology (NPT)
- FineSim SPICE (Full SPICE with NPT)
  - Increased analog SPICE capacity
  - Single-CPU FineSim SPICE 3-10X Faster Than Other SPICE Engines
- FineSim Pro (Fast SPICE with NPT)
  - 1-3% SPICE Accuracy

**Integrated Analog Simulation Environment**

- FineSim Customer Success
  - Toshiba, Maxim, Faraday, AMD, SiliconBlue, STARC, Sigma Design...
Fully Integrated Custom/Digital Analysis

- **Sign-off Quality Analysis**
  - DRC, LVS
  - Extraction, Timing
  - Noise, Power
  - DFM, Yield

- **Complete Integration**
  - Push-button “invocation”
  - Cross-probing debug
  - Fast incremental iteration
Unified, Shape-Based Custom & Chip Finishing Router

- Shape-based flexibility
- Built for modern nm geometries and design sizes
- Supports Schematic driven Layout
  - Custom routing constraints
- Automates critical signal handling
  - Net length control (min, max, match T-line)
  - Signal shielding (parallel, tandem, coax)
  - Differential pair support

- Analog-digital global routing
  - Ensures timing consistency across digital and custom routing regions
  - Speed and capacity to easily handle the largest mixed-signal chips
Titan: Open Architecture

- GDS
- Volcano
- LEF / DEF
- Verilog
- Live Link

PDK

3rd Party Tools

PCells™ / PyCells™

OA

GDS

SPICE

Live Link
Analog IP Design & Process Migration

IP process migration requires almost as much circuit design and layout time as the original rev!

Modern Approach to Analog IP Process Migration

- Write a specification on a computer
- Analyze the resulting circuit
- “Implement and Optimize” it
- Re-Use it
  - Change specifications
  - Change process nodes
  - Do in minutes what would take days and months “the old way”
Titan

Integrated Simulation (FineSim)

Mixed Signal Physical Constraints

Schematic / Layout Editor

AnalogWare

Standard

Custom

Matlab Specs

Titan Analog Optimization (Circuit & Physical)

Process Models

Process Compiler

Sized and Verified Design

PDK

Revolutionary Analog IP Design & Process Migration
# Titan: Process Migration Results

<table>
<thead>
<tr>
<th>Description</th>
<th>Without Titan AO</th>
<th>With Titan AO</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI-E IO driver, 2.5GHz (17 corners)</td>
<td>2 weeks</td>
<td>1 hour</td>
</tr>
<tr>
<td>Bandgap (33 corners)</td>
<td>3 weeks</td>
<td>5 min</td>
</tr>
<tr>
<td>6.4GHz SERDES Linear Equalizer (9 corners)</td>
<td>2 weeks</td>
<td>5 min</td>
</tr>
<tr>
<td>1.5GHz, 1V PLL (9 corners)</td>
<td>2 months</td>
<td>1 hour</td>
</tr>
<tr>
<td>12 bit pipeline, 100MS, system + op-amps (5 corners)</td>
<td>2 weeks</td>
<td>1 hour</td>
</tr>
</tbody>
</table>

Order Of Magnitude Faster Porting While Achieving Equal Or Better Performance
Titan: Integrated Mixed-Signal Platform

- **Mixed-Signal Platform**
  - Embedded Talus
  - Shape-Based Routing
  - Mixed-Signal Verification

- **Analog Block**
  - Design & Migration

- **Speed and Capacity**

- **Compatibility**
  - Accommodate legacy data
  - OA Compatible