What is needed under the hood of Nanotechnology...

Shekhar Borkar
Intel Corp.
Feb 10, 2007
Outline

Evolution of Electronics to CMOS

The three tenets

Technology outlook

Challenges

Potential solutions

Summary
Evolution of Electronics

- 1850: Mechanical
- 1875: Electro-Mechanical
- 1900: Electronic-VT
- 1925: Bipolar
- 1950: NMOS
- 1975: CMOS
- 2000: 
- 2025: ?

All cross-road technologies show:
1. Gain
2. Signal/Noise
3. Scalability

Performance
Energy
Price/Performance
The Three Tenets

(1) Gain

(2) Signal/Noise

(3) Scalability, in some shape or form
Electro-Mechanical scaling—Relays

1928, Otis Elevator
Vacuum Tubes

1920’s

1930’s

ST, UX base  Globe, UV base  Globe, UX base

1950’s & 60’s
Semiconductors

The first transistor

The first integrated circuit

4004

Pentium® 4
Benefits of Scaling

- **Cubic Meter**
  - Vacuum tube
  - Transistor
  - NMOS
  - CMOS

- **Delay (Sec)**
  - Vacuum tube
  - Transistor
  - NMOS
  - CMOS

- **Joules**
  - Vacuum tube
  - Transistor
  - NMOS
  - CMOS

- **Cost ($)**
  - Vacuum tube
  - Transistor
  - NMOS
  - CMOS
# Technology Outlook

<table>
<thead>
<tr>
<th>High Volume Manufacturing</th>
<th>2004</th>
<th>2006</th>
<th>2008</th>
<th>2010</th>
<th>Technology Node (nm)</th>
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<td>Technology Node (nm)</td>
<td></td>
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<td>Integration Capacity (BT)</td>
<td>2</td>
<td>4</td>
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<td>&gt;0.35</td>
<td>&gt;0.5</td>
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<td>Bulk Planar CMOS</td>
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<td>Alternate, 3G etc</td>
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<td>Metal Layers</td>
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<td>7-8</td>
<td>8-9</td>
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CMOS Research Continues...

- **Si Substrate**
- **Metal Gate**
- **High-k**
- **Tri-Gate**

**Technology Generation**
- **90 nm** 2004
- **65 nm** 2006
- **45 nm** 2008
- **32 nm** 2010
- **20 nm** 2012+

**SiGe S/D**
- Strained Silicon

**Manufacturing**
- **50 nm**
- **35 nm**
- **30 nm**
- **20 nm**
- **10 nm**

**Development**
- Nanowire

**Research**
- Carbon Nanotube FET
## CMOS—Cross Road?

<table>
<thead>
<tr>
<th>Cross Road False Alarms</th>
<th>1 μm</th>
<th>0.5 μm</th>
<th>130 nm</th>
<th>65 nm</th>
<th>22 nm</th>
<th>…</th>
<th>&lt; 1.5nm</th>
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<tr>
<td>Short Channel Effects</td>
<td>Device</td>
<td>Interconnects</td>
<td>More metals, Cu Low K ILD</td>
<td>Leakage control, avoidance, tolerance</td>
<td>Hi-K + Metal Gate</td>
<td>EUV, Self assembly</td>
<td>SD Tunneling</td>
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<td>Device Engineering</td>
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<tr>
<td>Gate Leakage</td>
<td>Leakage control, avoidance, tolerance</td>
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<td>Interconnects</td>
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What’s in sight after CMOS?

Which technology shows gain?

Satisfactory signal to noise ratio?
• At room temperature?

Scalability in some shape or form?
• Performance, Energy, Cost

Research must continue to find one

Then it will take 10-15 years to mature

Until then…

CMOS will continue…
...But With Challenges!

Random Dopant Fluctuations

Sub-wavelength Lithography

Heat Flux (W/cm²)—Vcc variation

Temp Variation & Hot spots

Source: Mark Bohr, Intel
Yesterday’s Freelance Layout

No layout restrictions
Transistor orientation restricted to improve manufacturing control
Transistor Width Quantization
Today’s Unrestricted Routing
Future Metal Restrictions
Reliability

Soft Error FIT/Chip (Logic & Mem)

Time dependent device degradation

Extreme device variations

Burn-in may phase out...?
Implications to Reliability

Extreme variations (Static & Dynamic) will result in unreliable components

Impossible to design reliable system as we know today

• Transient errors (Soft Errors)
• Gradual errors (Variations)
• Time dependent (Degradation)

Reliable systems with unreliable components — Resilient μArchitectures
Implications to Design & Test

Design with regular fabric

One-time-factory testing will be out

Burn-in to catch chip infant-mortality will not be practical

Test HW will be part of the design

Dynamically self-test, detect errors, reconfigure, & adapt
In a Nut-shell...

100 Billion Transistors

100 BT integration capacity
Billions unusable (variations)
Some will fail over time
Intermittent failures

Yet, deliver high performance in the power & cost envelope
Recipe for Resiliency

1. Detect
2. Isolate
3. Confine
4. Reconfigure
5. Recover & adapt

1. Circuit
2. Firmware
3. Platform
4. Software
5. Application
Resiliency with Reconfiguration

- Dynamic on-chip testing
- Performance profiling
- Spare hardware
- Binning strategy
- Dynamic, fine grain, performance and power management

Dynamically...
1. Self test & detect
2. Isolate errors
3. Confine
4. Reconfigure, and
5. Adapt

Coarse-grain redundancy checking
Dynamic error detection & reconfiguration
Decommission aging HW, swap with spare
## Shifts towards the Nano-era

<table>
<thead>
<tr>
<th>From</th>
<th>To</th>
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</thead>
<tbody>
<tr>
<td>Deterministic design</td>
<td>Probabilistic design</td>
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<tr>
<td>Local optimization</td>
<td>Global optimization</td>
</tr>
<tr>
<td>Irregular, free-lance design</td>
<td>Regular design fabric</td>
</tr>
<tr>
<td>Reliable components</td>
<td>Reliable systems with unreliable components</td>
</tr>
</tbody>
</table>

*Time will be just ripe then for Nano-technology*

Do not try to mimic CMOS with Nano-technology

(Imagine trying to build Babbage’s difference engine with CMOS)

Invent a new theory of computation
Why Bother?

Litho Cost

- $100,000
- $10,000
- $1,000
- $100
- $10
- $1

- 1960
- 1970
- 1980
- 1990
- 2000
- 2010

G. Moore
ISSCC 03

FAB Cost

- $10,000
- $1,000
- $100
- $10
- $1

- 1960
- 1970
- 1980
- 1990
- 2000
- 2010

www.icknowledge.com

$ per Transistor

- 1.E-06
- 1.E-05
- 1.E-04
- 1.E-03
- 1.E-02
- 1.E-01

- 1960
- 1970
- 1980
- 1990
- 2000
- 2010

$ per MIPS

- 1.E+04
- 1.E+03
- 1.E+02
- 1.E+01
- 1.E+00
- 1.E-01
- 1.E-02

- 1960
- 1970
- 1980
- 1990
- 2000
- 2010
Summary

Three tenets: Gain, Signal/Noise, Scalability

Nothing on the horizon yet that satisfies them

But research must continue to find one

Probably a lot different than CMOS—don’t try to mimic CMOS!

Several challenges lay ahead, but when have they not?