Analysis and Design of High-Speed Interconnects

Cheng-Kok Koh
School of Electrical and Computer Engineering
Purdue University

Chengkok@ecn.purdue.edu
http://www.ece.purdue.edu/~chengkok
Outline

- Interconnect challenges
- Inductance extraction
- Twisted-bundle layout structure
- Future directions
Interconnect challenges

- Interconnect delay
  - Interconnect delay dominates gate delay
- Delay variation
  - Capacitive coupling
  - Inductive coupling
- Signal integrity
  - Capacitive and inductive couplings
  - Decreasing supply voltage
Inductance formulas

- Parallel filaments
  \[ M = \frac{\mu}{2\pi} \left[ \ln \left( \frac{l}{d} + \sqrt{1 + \frac{l^2}{d^2}} \right) - \sqrt{1 + \frac{d^2}{l^2} + \frac{d}{l}} \right] \]

- Geometry Mean Distance (GMD)
  - Pre-computed tables

- Exact formula for self and mutual inductances
  - C. Hoer and C. Love, 1965
  - Numerically unstable
Numerical instability of Hoer and Love’s formula

Self-inductance:

![Graph of Self-inductance](image)

Mutual-inductance:

![Graph of Mutual-inductance](image)
New exact formula: Virtual wires
Mutual inductance

- Mutual inductance in terms of self-inductances of virtual wires

\[
M = \frac{1}{W_0 T_0 W_1 T_1} \frac{1}{8} \sum_{i_0, i_1, j_0, j_1, k_0, k_1 = 0}^1 (-1)^{i_0 + i_1 + j_0 + j_1 + k_0 + k_1 + 1} A^2 L_{p_{i_0 j_0 k_0} q_{i_1 j_1 k_1}}
\]

- Numerically stable exact closed-form formula for self-inductance exists [Ruehli, IBM’72, Wu-Kuo-Chang, Tmicrowave’92]
Numerical results

- Mutual inductance
  - Cross-section: 0.5 \( \mu \text{m} \times 1 \mu \text{m} \)
  - Separation: 1.5 \( \mu \text{m} \)
  - Length: varies
Our formula
C. Hoer and C. Love’s formula
Modified FastHenry

Self-inductance:

Mutual-inductance:
Skin Effect Example

Inductance (H) vs. Frequency (Hz)

- Our tool
- FastHenry
Mutual Inductance
Twisted bundle layout structure

- Motivation and construction
  - Twisted-pair
  - Loop inductance based
  - Synthesis of ground line and signal lines simultaneously
  - Re-ordering of wires to reduce inductive coupling

- Verification
  - PEEC based
  - Consider P/G mesh
Twisted-pair structure

\[ M = \left( \int \int B \cdot d\bar{S}_{s21} + \int \int B \cdot d\bar{S}_{s22} \right) / I_1 \]

\[ = \left( \int \int B \cdot d\bar{S}_{s21} - \int \int B \cdot d\bar{S}_{s21} \right) / I_1 \]

\[ = 0 \quad \text{Zero coupling inductance} \]
Multiple-signal bus

- ground
- signal 1
- signal 2
- signal 3

Twisted group

Normal group
Current loops due to signal 2

ground

signal 2

loop21

loop22

loop23

loop24
16-bit twisted-bundle bus

Twisted group

normal group

Twisted group

normal group
Stick diagram of the layout

NOT drawn to scale
Normal structure
Experiment setup

- Wire length: 1mm, 2mm, 4mm
- driver: 160X, receiver: 40X
- $1.5V \ V_{dd}$
- PEEC model
Power/Ground Grid

P/G Pitch: M6, 150µm; M5 50µm
P/G Width: M6 60µm; M5 10µm
P/G Pad Pitch: 300µm
Signal Pitch: 1µm
Signal Width: 0.5µm
Wire Thickness: 1µm
Noise Comparison (1mm, 1GHz)
Future Directions

- Inductance extraction:
  - Double inversion in frequency-dependent inductance extraction too costly
  - Substrate conductivity
- Fast simulation and analysis
  - Reduced order modeling
  - Exploit the sparsity of $L^{-1}$
- Interconnect optimization
  - Signal-to-power ratio
  - Shield width, signal width, separations