User Programmable Logic Device: Architecture and CAD Tools

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Design Decisions

- Mid-size Capacity
  - For control logic
- Hierarchical Interconnection Structure
  - Predictable delay
- PLA-based Cell Structure
New Architecture

- Cell Structure
- Interconnection Architecture
Single-Output PLA Cells

- Investigate the tradeoff between chip area/delay and cell granularity for single-output PLA cells.
Conclusions for Cell Structure

- Area model:
  3-4 inputs, 2 products

- PLA-based FPGA area versus cell granularity by Kouloheris and Gamal:
  8-10 inputs, 12-13 products, 3-4 outputs

- Area model plays an important role in the architecture evaluation process
Interconnect Architecture

PI = 6

PO = 6

S = 2

level 1

level 2

level 3

level 4

A

B

A

B

12

1234
Hierarchical Interconnect Structure

- switch
- logic cell
Graph Model of Interconnections

- **input**
- **output**

- cell1 cell2 cell3
- pin1 pin2

- Level1_input
- Level2_input
- Level3_input

PI
Development Flow

- **Input**
- **Technology Mapping**
  - TV-Pack
  - U of Toronto
- **Hierarchical Clustering**
  - Hierarchical clustering for area
- **Placement & Routing**
  - SIS-TEMPLA
  - Performance driven hierarchical clustering
- **Output**
  - Placement & 100% routing completion
Algorithm for Technology Mapping

- Area minimization and Delay (Depth) minimization

Single-output PLA blocks
Hierarchical Clustering for Area

Given pin and capacity constraints of block at each level, minimize the area required (the number of top-level blocks)
Min-Cut Based Hierarchical Clustering

- **Step 1**: Min-cut (net) based K-way partition by hMetis (initial partition)
- **Step 2**: Refine the initial partitions to satisfy pin and area constraints.
- **Step 3**: If pin and area constraints can’t be satisfied, then abort, re-start and set K=K+1.
- **Step 4**: If it reaches leave block, then outputs the result else do the next level partition
Performance Driven Hierarchical Clustering

- Given timing constraint (required time), pin and block capacity constraints, Minimize the area required (the number of top blocks)
Algorithm

1. Clustering
   - Labeling
   - Multiple fan-out node duplication

2. Merging
   - 3-Level hierarchical merge
   - Area constraint
   - Pin constraint
## Delay & Area Comparisons

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Placement and Routing

Clustering Net-lists

architecture file → placement & routing on graph → P & R output
Algorithm for Placement and Routing

- While( not all nodes placed )
- {
  - pick the most critical net-list from the net-list set;
  - for the selected net
  - do
  -   compute priority of node for the selected net;
  -   select one node based on node’s priority;
  -   select location for the node based on the current placed nodes;
  -   place the node at the selected location;
  -   update priority of nets;
  -   mark placed nodes;
- }
Future Work

- Architecture Study
  - Area
  - Speed
  - Expandability
- Design Tools
  - Technology Mapping
  - Placement and Routing