IC–SOC
Design Drivers Update

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Network Processing

Physical Layer → Network Processing Functions → Switching

Framing → Verification Classification → Modification → Encryption Compression → Traffic Queuing
Proposed NP

ROM

CPU

DSP

FPGA

DRAM

SRAM

Switch Fabric

Flash

8Kx16 SRAM Core

20 M26 Switch Pile Core

drivers1.03/cww

DTC, NTHU
Cores

- **CPU**: PKU (X Cheng)
- **DSP**: NTHU (YL Lin)
- **SRAM/ROM/Flash**: NTHU (CW Wu & YL Lin)
- **DRAM**: Industry
- **FPGA**: UCLA (J Cong)
- **CP**: NTHU (YL Lin & CW Wu)
- **On-Chip Bus**: UCSB/NTHU (KT Cheng & CW Wu)
- **LBIST**: UCSB (KT Cheng)
- **MBIST**: NTHU (CW Wu)
DTC Project: NP (NSC)

Main Project NP

- System Integration
- Chip Planning
- Debugging
- Diagnosis
- Formal Verification
- DFT BIST
- Testing

Subproject 1:
- Allen Wu

Subproject 2:
- T.-Y. Chang

Subproject 3:
- S.-Y. Huang

Subproject 4:
- C.-W. Wu
DTC NP Architecture

嗪Target: base-band coding for network communication

• Source coding
• Channel coding
• Crypto-processing

馍Major IP cores: COP, ACP, DSP, SRAM

馍On-chip bus: AMBA
Communications Processor (COP)

- A 32-bit RISC processor
- Source coding and channel coding for communication
- Capable of finite field operation
- Central controller of system
Asymmetric Crypto-Processor (ACP)

- A processor-based RSA encryption/decryption engine
- Capable of modular multiplication operation
- EC, DES, & AES being considered
AMBA

- Advanced Microcontroller Bus Architecture
- Standard system bus for ARM-based chip
- Open standard for SOC on-chip bus
  - Flexible and suitable for a wide range of SOC applications
Memory Cores

- **SRAM**
  - Global UniChip Corp. (GUC) & TSMC
  - DTC-GUC projects
  - Chip Implementation Center (CIC)
  - NSC projects

- **Flash memory**
  - MXIC
  - DTC-MXIC projects