Development of a low-power GOPS embedded DSP core for communication and consumer information appliances

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Goals

- 32-bit RISC + 16-bit DSP, 24-bit Inst Format
- Core Density + Low Power
- Dual Issue, 5-Stage Pipeline, SIMD ALU
- Dual (or Quad) MAC, Dual DM(DSP AGU), Zero-Overhead Loop
- FF-based, Synthesizable
- > 1 BOPS, < 0.1mW/MHz @ 0.18um
Processor Design (Progress Report 2000/8-2001/7)

- Instruction Set Design and Evaluation
- Architectural Design
- RTL Implementation in Verilog
- Synthesis to 0.35um CMOS
- Preliminary Performance Evaluation

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Why a new architecture?

- IA Applications
- Why not a compatible? (ARM, MIPS, ADI)
- Why RISC+DSP?
- Chance of Success?
- Software Issues
- Open Core Policy