

Physical Synthesis for Power Under Process Variation

Jason Cong (UCLA CS Dept. cong@cs.ucla.edu, (310)206-2775) and Tony Chan (UCLA Math Dept. chan@math.ucla.edu)

Motivation The most significant progress in EDA in the past ten years is arguably the development of physical synthesis technology and its wide adoption by the IC design industry today. However, the existing physical synthesis technology has several limitations: (1) It was originally developed to address the “timing closure” problem, thus, did not give sufficient consideration of power optimization. Although a number of power optimization techniques have been added in many physical synthesis flows (such as cell sizing, multiple Vt and Vdd selections), there is lack of general and efficient algorithmic framework to consider and balance all available power optimization opportunities, especially in connection with placement. (2) It did not consider increasing *process variations* in nanometer designs, therefore, the results by existing physical optimization algorithms may not work under all “*timing corners*”. A considerable “safe margin” is added to guard-band the statistical variation, resulting in a sizable waste of power, area, and performance.

Objectives

- (a) Develop a unified and efficient mathematical foundation and algorithmic framework for physical synthesis to support power optimization guided by *both* physical locality *and* an evolving netlist structure. For example, the placement engine should support multi-Vdd islands, clock gating and power gating, where physical locality has a big impact on optimization quality. But it should also support cell sizing, buffering, logic structuring, where an *evolving* netlist and thus changing logic density need to be considered, *during* placement, for correct power optimization.
- (b) Develop efficient theory and algorithms to support *statistical optimization* under process variation so that the physical synthesis results satisfy all timing constraints under *all timing corners* or achieve the required *timing-yield constraints* under given probability density functions (PDFs).
- (c) Consider the efficient use of multi-core CPUs (as they become widely available) to further improve the runtime efficiency for coping with the high complexity of the proposed problem.

Technical Approaches Our initial thinking leads to several directions.

- (1) We believe that multilevel/multiscale optimization will be a good candidate for providing a unified algorithmic framework for physical synthesis for power under variation, as we have demonstrated in our current SRC project that it is an efficient framework for large-scale placement under complex constraints [Chan05] and successfully influenced its adoption by the placement community (e.g. [Hu05, Kahng05, Vorwerk05]);
- (2) We shall make use of the recent mathematics research in optimization under uncertainty. For example, it was shown that for certain problem classes, it is possible to minimize a given objective over *all* possible realizations of the constraints and thus guarantee feasibility of the computed solution (“robust optimization” [Ben-Tal98, Ben-Tal00]). For other classes, including realistic circuit-design, PDFs are used either to maximize the probability of obtaining a feasible solution or to enforce a lower bound on this probability (“chance-constrained optimization” [Charnes59]). Still others are amenable to deterministic optimization of a randomly selected sample realization of the problem followed by refinement, if necessary; to satisfy analytically derived bounds on the maximum proportion of violated constraints [Calafiore05]. Most work to date has been limited to linear and convex problem formulations. We will extend the theory and algorithms as needed to fit our applications.
- (3) We will leverage the extensive research on power optimization techniques (e.g. [Bahar01, Borkar01, Brodersen02, Chandrakasan95, Cong94, Correale95, Singh95, Wang98, Wei98]) and recent work on statistical optimization in circuit designs, such as statistical-optimization-based gate sizing [Agarwal05, Bai02, Mani05, Singh05a], technology mapping [Singh05b] and power-and-ground network design [Boyd01]. The main challenges are (i) to integrate them in a unified algorithmic framework, so that we can consider the trade-off of various optimization techniques under PDFs or multiple timing corners, and (ii) to extend these techniques to placement and placement-based optimization, where there exists large number of nonconvex nonoverlap constraints.

It is almost certain that more interesting ideas will emerge as we start our investigation, as we have consistently demonstrated in the past.

Anticipated Results of the proposed research include technical reports, published papers in major EDA conferences and journals, and a software prototype of a novel physical synthesis flow for power optimization under process variation. Our research group has a strong track record in delivering the results and transferring the technology to the SRC companies – our latest SRC project on placement (ending June’06) promised a Moore’s law generation reduction of wirelength (30%) and we already exceeded that goal considerably [Chan05].

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References and PI Bios <http://cadlab.cs.ucla.edu/cpmo/wp06refs.html>.