EDA
Past, Present & Future

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DEDICATED TO

Donald O. Pederson
A. Richard Newton

EDA Pioneers
The Beginning

- **Circuit Simulation**
  - Circuit Simulators in the 60’s
  - SPICE in the 70’s

- **Circuit Layout (Physical Synthesis)**
  - Lee Maze Router 1962
  - Breuer book 1972
    Design Automation of Digital Systems
The Best of ICCAD

- Functional Verification
- System Design and Analysis
- Logic Synthesis
- Analog and Digital Circuit Design
- Physical Simulation and Analysis
- Physical Design
- Timing, Test and Manufacturing
- Industry Viewpoints
Physical Design Classical Problems

- Routing
- Placement
- Partitioning
- Floor-Planning (Sequence Pair)
Timing Issues

- Delay
- Signal Integrity
- Modeling and Timing Analysis
- Timing-Driven Placement
- Interconnect Delay
- Wire Placement?
Outline

- Circuit Simulation
- Cadence - Chi-Ping Hsu (Corp VP)
  Power issue
- Nannor - Wayne Dai (Chairman and Founder)
  DFM issue
- Conclusions
Circuit Simulation

- Story of SPICE
- Ron Rohrer: CANCER (Computer Analysis of Nonlinear Circuits Excluding Radiation)
- Don Pederson: SPICE (Simulation Program with Integrated Circuits Emphasis)
- Larry Nagel
- Rich Newton
SPICE 2 1975

- Modified Nodal Analysis
- Dynamic Memory Management
- Multiple-Order Integration Method of Gear
- Time-Step Control Algorithm
- More Accurate MOS Models
- Secondary Effects for BJT's
SPICE 3 1985

- Interactive Program
- Modular Version in C of SPICE 2
- Graphic Display of Results
- Basis for New Circuit Simulation Developments at UC Berkeley
SUBSEQUENT SIMILATORS

- Semi-Implicit Integration: MOTIS 1975
- Relaxation: SPLICE 1984
- Waveform Relaxation: RELAX 1984
- Exponential Integration: XPSIM 1988
- Stepwise Constant Device Model: SPEC 1989
- Asymptotic Waveform Evaluation: AWE 1990
- Step Wise Equivalent Conductance: SWEC 1992
Digital MOS Circuits with Transmission Lines

**Key Features**

- Stepwise Equivalent Conductance Model
- Event-Driven Approach Based on Slopes
- Pade’ Approximation and Recursive Convolution
Model Order Reduction

- Pade: Explicit Moment Matching
- Balanced Truncation
- Chebyshev Polynomial
- State Space:
  - Krylov Subspace and Arnoldi Algorithm
  - Congruent Transformation and Passivity
- Variational Interconnect Model and Stochastic Approach
Commercial Software

- Device and Interconnect Models
- Partitioning
- Model Order Reduction
- Multi-rate and Event driven Simulation
- Hierarchical Simulation
Commercial Software
Star-Sim, Hsim, UltraSim

- Digital, Analog and Mixed Signal
- Power, Delay, Noise and Reliability
- Speed: 100-1000 faster than SPICE
- Unlimited Capacity
What is UltraSim?

- *Fast SPICE*” Hierarchical Simulator
  - Transistor-level full-chip dynamic simulator
  - For SoC, Memory, Digital Logic & Mixed-signal
  - 100 to 1,000 times faster than SPICE
    - In flat mode
    - Has capacity to handle multi-million transistors
      Circuit with accuracy that is within 2-3% of SPICE
  - 1,000 to 1,000,000 times faster than SPICE
    - In hierarchical mode
    - Remains within 2-3% of SPICE
Circuit Analysis Research with UCSD

- Generalized Y-Delta Transformation for Circuit Reduction
- Integration Methods
  - Alternating Direction Implicit Method (Two-way Partition)
  - Exponential Operator Splitting Method (Multi-way Partition)
- Linear System Solutions
  - Two-Stage Newton Raphson Iteration
  - AMG for linear sub-circuits
  - KLU for nonlinear sub-circuits
- Distributed Simulation
Distributed Simulation Process

- Distributed Circuit Partitioning
  - Two-Stage Newton-Raphson Partition
  - Domain Decomposition
- Distributed Device Loading
- Fast Parallel Matrix Solver
  - Iterative Matrix Solver on Linear System
  - Distributed Direct Solver on Partitioned Subcircuits
- Homotopy Nonlinear Solver
- Adaptive Time Step Control
Simulation for the Future

- Mems (Kris Pister)
- Bio (Shankar Sastry)
- Optical
- Nano
Cadence Design Systems
Global leader of design automation solutions

Market Cap: $5.5B*
2006 Revenue: $1.5B
WW offices: 57
Employees: 5200

*February 2007

North America 54%
Europe 19%
Asia 10%
Japan 17%
MISSION

To be and be recognized as the indispensable partner to the electronics industry

Cadence Design Systems
Enabling companies to play in trillion dollar markets...
Semiconductor consumption driven by 3 ‘Cs’

Consumer. Computing. Communications

2004-2009 Total IC Market by System Type ($B)

Source: SIA, IC Insights
Design chain orchestration

Biggest investment in collaboration with your design chain partners

Test chips
Reference Flows
Joint development
Methodologies
Thought leadership

Si2 to facilitate standardization of the Common Power Format (CPF) through the IEEE

power forward™
Industry wide Common power format
Process migration is creating new power management challenges
Current design-based solutions are fragmented

Logic is “Connected”

Power is Not “Connected”

Can be Automated

Very Difficult to Automate
## Impacts of Advanced Low-power Techniques

<table>
<thead>
<tr>
<th>Power reduction technique</th>
<th>Leakage power</th>
<th>Dynamic power</th>
<th>Timing penalty</th>
<th>Area penalty</th>
<th>Implement. impact</th>
<th>design impact</th>
<th>verification impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Area optimization</td>
<td>1.1X</td>
<td>10%</td>
<td>0%</td>
<td>10%</td>
<td>Low</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>Multi-Vt optimization</td>
<td>6X</td>
<td>0%</td>
<td>0%</td>
<td></td>
<td>Low</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>Clock gating</td>
<td>0X</td>
<td>20%</td>
<td>0%</td>
<td>&lt;2%</td>
<td>Low</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>Advanced</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Multi-supply voltage (MSV)</td>
<td>2X</td>
<td>40-50%</td>
<td>0%</td>
<td>&lt;10%</td>
<td>Low</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>Power shut-off (PSO)</td>
<td>10-50X</td>
<td>~0%</td>
<td>4-8%</td>
<td>5-10%</td>
<td>Low</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>Dynamic and Adaptive Voltage Frequency Scaling (DVFS and AVS)</td>
<td>2-3X</td>
<td>40-70%</td>
<td>0%</td>
<td>&lt;10%</td>
<td>Low</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>Substrate Biasing</td>
<td>10X</td>
<td>-</td>
<td>10%</td>
<td>&lt;10%</td>
<td>Low</td>
<td>None</td>
<td></td>
</tr>
</tbody>
</table>

*Automated in the 1990’s*
Si2 Low Power Coalition Forms to Unify Standardization Efforts

- LPC Members Announced (17)
  - IBM
  - Intel
  - Texas Instruments
  - STMicroelectronics
  - AMD
  - NXP Semiconductors
  - LSI Logic
  - Cadence Design Systems
  - Magma Design Automation
  - Sequence Design
  - Apache Design Solutions
  - Atrenta
  - Azuro
  - Virage Logic
  - ChipVision Design Systems
  - Golden Gate and others
"Yes, you need to do DFM at 65 nm. By 65 nm we cannot eliminate systematic yield losses with anything we can do in the foundry. It's up to the chip-design teams."

- David Lan, TSMC North America
Sources of Yield Loss

- **Lithography**
  - the feature sizes are decreasing faster than exposing wavelengths
  - Layout geometries by the design tools ≠ Actual geometries on the wafer

- **Random Particles**
  - Extra metal defects → bridge faults
  - Missing metal defects → open faults

- **Interconnects**

- **And more…**
Resolution Enhancement Techniques (RET)

- Resolution Enhancement Techniques (RET)
  - Optical proximity correction
  - Scattering bars
  - Phase shift masks (PSM)

- However
  - Determining the RET patterns is complex and context-dependent → higher cost
  - Increases the complexity of the geometry → lower mask yield → higher cost
Spacing/width Optimizations

- Wire spreading
  - Move wires apart with an optional extra spacing
- Wire widening
- DFM guideline
Yield-preferred Vias

- **Redundant-cut via:**
  - at least one redundant cut
  - not required in functionality
  - reduce via failure

- **More metal coverage**
- **DFM guideline**
Conventional Techniques Fails

- **Fight with yield loss:**
  - Recommended DFM rules
  - DFM guidelines

- **Number and complexity of design rules are exploding**

- **Design rules cannot cover all the manufacture issues**

- **Routers can’t handle the complex rule set efficiently**
  - Slower (more rules)
  - More chip area (overhead)
**Nannor’s Solution: Acuma™**

- **Stand-alone from the main flow**
  - More flexible
  - More versatile
  - More capable
- **Plug-in and play**
  - Compatible with all design flows
- **Interface with DFM analysis tools**

Diagram:
- Floorplan
- Placement
- Routing
- Timing Verification
- Advanced Design Rules
- Litho Analysis
- Critical Area Analysis
- Milkyway
- OA
- LEF/DEF
- Lava ...

- Acuma™
Provide efficient layout modification for advanced design rules.
Enable advanced design rule implementation with reduced turn-around-time and full-chip capacity.
Support local rip-up and reroute.
Have 1 US patent granted and 3 US patents pending.
CONCLUSION

- Circuit Simulation
  - Distributed Computing
  - Stochastic Approach
  - Application to other Areas

- DFM
  - Power Forward
  - Yield-Oriented Physical Design