Research Progress on Power/Ground Network Design and Optimization for SOC

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Xianlong Hong

Dept. Of Computer Science & Technology, Tsinghua University, Beijing
Motivation

- Power/Ground network design is a very important part in VLSI design
- Improper Power/Ground network design affects the performance of circuit
  - Functional error and lower switch speed caused by excessive voltage drop
  - Undesirable wear-out of metal wiring caused by electromigration (excessive current density)
Problem Formulation

Minimize: \[ a = \sum_{(p,q)\in \mathcal{E}_{bch}} l_{pq} w_{pq} = \sum_{(p,q)\in \mathcal{E}_{bch}} \rho_{pq}^2 g_{pq} = \sum_{(p,q)\in \mathcal{E}_{bch}} \alpha_{pq} g_{pq} \]

Subject to:

\[ v_i \geq v_{dd} - u \quad \text{for all } i \in E_{\text{leaf}} \] (voltage drop constraint)

\[ |v_p - v_q| \leq \rho_{pq} \sigma \quad \text{for all } (p,q) \in E_{\text{bch}} \] (current density const.)

\[ \sum_{q \in E_{\text{net}}(p)} (v_q - v_p) g_{pq} = i_p \quad \text{for all } p, q \in E_{\text{node}} \] (Kirhoff law const.)

\[ w_{pq} \geq w_{\text{min}} \quad \text{for all } (p,q) \in E_{\text{bcl}} \] (min. wire width const.)
Topology of P/G Networks

- **TREE**
  - BBL Layout Mode
- **MESH**
  - Standard Cell Layout Mode
- **GENERAL GRAPH**
  - All Layout Mode
Main Steps of P/G Network Design

1. Construct a Topology

2. Minimize Wiring Area

3. Verify Feasibility

Heuristic Searching Method

Mathematical Programming
Completed Projects

- Power/Ground Network Design and Optimization for BBL Mode
- Power/Ground Network Design and Optimization for Cell Based Layout Mode
- PECT: Area Minimization Algorithm of Power/Ground Network based on Nonlinear Programming Technique for the General Graph Mode
Power/Ground Network Design and Optimization For BBL Mode
Phase 1: P/G routing
- To solve Minimum Current Tree Problem (MCT)
- MCT = minimum (current * length) tree
- A path of MCT from leaf node to root node must be the shortest path from leaf node to root node

Phase 2: P/G wire sizing
- For tree structure current directions of all branches are fixed and all constraints are linear.
- To use Lagrangian Relaxation Method (LRM) to solve convex programming
Program Step 1
— P/G Routing using MCT technique

ami33

ami49
Program Step2
— P/G wire sizing using LRM

Power Trees of ami33

Power Trees of ami49
## Experiment Results

<table>
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<tr>
<th>circuits</th>
<th>wiring area using the same width ($\mu m^2$)</th>
<th>optimized wiring area ($\mu m^2$)</th>
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Power/Ground Network Design and Optimization for Cell-Based VLSIs with Macro Cells
Mesh-based Network with Ring

- Basic Row Power Rail
- Power Straps
- Peripheral Power Bus

- GND
- VDD
- Power Ring
- Macro Cell Power Pin

- R1
- R2
- R3
- R4
- R5
- R6
Problem of Macro Cell

current of macro cell is known + current of macro cell’s pins is known

meet all current distribution of the macro cell’s pins

Kirchoff’s Law
Power Ring Constraints

Voltage Drop
Electromigration

$S : \text{Searching Space} = \star + \odot + \odot$

$Q : \text{Power Ring Constraints} = \odot$

How to prove $Q$ belongs to $S$?
Inclusive Theorem:

- S is a convex set, Q is a bounded convex set which has the finite polar points, N is the number of Q’s polar points, then

\[ I^{(1)}, I^{(2)}, \ldots, I^{(N)} \in S \Rightarrow Q \subseteq S \]

- obtain polar points of Q:
  - The kth vertex of Q is \((I_1 = 0, I_2 = 0, \ldots, I_k = I_{ring}, \ldots, I_N = 0)\)
## Experiment Results

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<tr>
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<th>area after optimization</th>
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PECT: Area Minimization Algorithm of Power/Ground Network Based on Nonlinear Programming Techniques for The General Graph Mode
Previous Work 1
Chowdhury-Breuer Algorithm


- **Main Points:**
  - Augmented Lagrangian function
  - Current is looked as variables

- **Problems:**
  - Redundant Searching Space
  - Equation constraints result in poor convergence

- **Scale of testing circuits**
  - no more than 20 branches
Previous Work 2
Mitsuhashi-Kuh Algorithm

- 29th ACM/IEEE Design Automation Conference 1992
- Main Points:
  - Feasible Direction Method + Linear Programming
  - Adjoint Network — Gradient of voltage subject to conduct
- Problems:
  - Inequation constraints — Zigzagging problem
  - Adjoint network — Requires too much time and memory
- Scale of testing circuits:
  - no more than 42 nodes
36th ACM/IEEE Design Automation Conference  1999
(Best Paper)

Main Points:
- A constrained nonlinear programming problem — sequence of linear programming
- Voltages and currents are also used as variables

Problems:
- Redundant searching space
- Optimization is divided into 2 steps — lost some searching space

Scale of testing circuits:
- About 10000 nodes
Solution Method

Penalty Method

1. Resize objective function
2. Update penalty parameter
3. Adaptive line searching
4. Advanced adjoint network

Conjugate Gradient Method

P/G solver

ICCG

5. Equivalent network
Key Techniques

- **Resize objective function dynamically:**
  - eliminate the difference between the objective function and penalty term

- **Update penalty parameter automatically:**
  - experiment results don’t depend on penalty parameter

- **Automatic Adaptive Line Searching:**
  - improve efficiency and precision of line searching

- **Advanced Adjoint Network:**
  - reduce time complexity of gradient calculation

- **Equivalent Network:**
  - decrease scale of node voltage equation set
Main Frame of PECT

1. Set initial point
2. Resize objective function
3. Unconstrained minimization
4. Violation
   - Yes: Update penalty parameter
   - No: End
Solving Time Versus Nodes Number

The graph shows the relationship between solving time (on the y-axis) and nodes number (on the x-axis). The solving time increases linearly with the nodes number.
Comparison of PECT with Tan-Shi Algorithm

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## Experiment Results of Larger Circuits

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PG2000: Power/Ground Network
Design, Optimization and Verification
Tool for Cell Based Layout Mode
User Interface of PG2000
Functional Blocks

Read LEF/DEF & Load Design

pg1: Verify P/G Design
pg2: Optimize P/G Trunk Num
pg3: Optimize P/G Trunk Width
pg4: Optimize P/G Trunk Area

Save P/G Design

Display Cells
Network Violation
Report Log
LEF/DEF Parameters
View Zoom
Zoom In
Zoom Out
Query Cells
Power Edge
Power Pin
Display Constraint Violation
## Experimental Result (1)

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Further Work

- Improve P/G network solver
- Improve nonlinear programming approach
- Multiple PAD and floating PAD problem
- Connect power estimation tool
Thank You!