C-based Design Methodology for Early Design Evaluation

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C-based Spec. for Early Design Evaluation

- Product definition
- Algorithm Selection
- C spec.
- Functional Evaluation
- Correct?

- Architecture Selection
- HW/SW Partitioning
- SW Spec.
- HW Spec.
- HW/SW Development
- System Integration
C-based Early Design Evaluation

- Functional verification
- Hard to assess the performance of hardware design
- Little support to architecture selection and design reuse
- What if we have a rapid design methodology that can:

  => automatically convert a C/HDL-based functional design spec. into an RTL design,

  => automatically exploit different architectures and reuse pre-designed cores, and

  => provide a HW/SW co-verification environment???
The Proposed C-based Design Methodology

Product definition

Algorithm Selection

C spec.

Functional Evaluation

Correct? No

C/HDL Spec.

XE

Arch. Exploration

Core Reuse

XD

RTL Design

Co-simulation & Co-emulation
The Co-Simulation Environment

- C-code
- GUI
- APL/FPL
- Simulator (ModelSim)
- RTL/gate-level
- PC-platform

Pentium III 450 X 2
256 MB
The Co-Emulation Environment

PC-platform
Software
- C-code
- Driver
- GUI
- Parallel port

Hardware
- FPGA board
- VIRTEXE-V1000-EHQ240
Main algorithm: computing object’s XYZ coordination with a given rotation direction and angel. It requires extensive floating-point multiplication computation.

Hardware/software co-design approach:
Hardware implementation: the floating-point matrix multiplication.
double* ___fastcall MatrixMultiply(float vector[64][4], float matrix[4][4]){
    double c[256];
    for(int i=0; i<=63; i++){
        for(int j=0; j<=3; j++){
            double tmp=0;
            for(int k=0; k<=3; k++){
                tmp = tmp + vector[i][k] * matrix[k][j];
            }
            c[i*4+j] = tmp;
        }
    }
    return (double*)c;
}
Synthesis Flow

C/HDL Spec. -> XE

RTL Spec. -> Xilinx FPGA Compiler -> Bit-Stream

32-bit Floating Adder 32-bit Floating Mult

XE <-> XD

Capturing

Xilinx Core Generator

16X32 RAM X 1
256X32 RAM X 2
Final FPGA Design

Clock Rate: 50MHz
Eq. Gate-count: 100,959
The Co-simulation/Co-emulation Environment
The Results

- C-based simulation: 64 frames/sec.
- C/RTL co-simulation: ~1 frame/30 sec.
- Co-emulation: 32 frames/sec.
SpecC vs. SystemC vs. C

- Will SpecC, SystemC or C become another hardware description language???

  => Most likely NO!!!

- C-based language may be good for system-level design exploration, functional simulation, rapid-prototyping, reconfigurable systems, and etc.

  => In this case, we should stick with C!!!

- C/C++ for software development and HDLs for hardware development