Proposal to National Science Foundation for Establishing an International Research Center on

Giga-Scale System-On-A-Chip Design

(Version 7 8/11/00)

Cover Sheet for Proposal to the National Science Foundation

1 Project Summary

This project proposes to establish an International Research Center on giga-scale system-on-a-chip (SOC) designs. It involves researchers from the U.S., Taiwan, and China. The proposed research activities include investigation and development of efficient SOC synthesis tools and methodologies, SOC verification, test, and diagnostic technologies, and an SOC design driver that motivates and validates various synthesis, verification, and test techniques developed during the course of this research project. We plan to use an SOC design of a network processor as the design driver, which includes embedded CPUs, DPSs, FPGAs, and various kinds of memory components. The research on SOC synthesis tools and methodologies includes design specification, design partitioning, synthesis and optimization for embedded DPSs and FPGAs, physical synthesis for full-chip assembly, and synthesis techniques for design re-use. The research on verification and test focuses on functional verification, self-test using on-chip programmable logic, analog and mixed-signal self-test, and test for embedded memories. The outcome of this research project will be innovative design methodologies, tools, and algorithms that enable efficient giga-scale SOC integration in nanometer technologies. The Center will also provide an excellent opportunity to train the next generation of young scientists because of the wide range of leading-edge research problems covered, as well as the unique international collaborative nature of this project. The requested funding from the National Science Foundation will be used to support researchers from the U.S. The Center is simultaneously applying funding from the National Science Council (NSC) in Taiwan and the Chinese National Science Foundation (CNSF) to support the proposed research activities of researchers from Taiwan and China, respectively. Additional funding from the NSF international program is also requested to facilitate international collaboration.
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3 Project Description

3.1 Introduction

The driving force behind the spectacular advancement of integrated circuit technology in the past thirty years has been the exponential scaling of the feature size, i.e., the minimum dimension of a transistor. It has been following Moore’s Law [1] at the rate of a factor of 0.7 reduction every three years. It is expected that such exponential scaling will continue for at least another 10 to 12 years as projected in the 1997 National Technology Roadmap for Semiconductors (NTRS’97) [2]. This will lead to over half a billion transistors integrated on a single chip with an operating frequency of 2-3 GHz in the 70nm technology by Year 2009. This enables system-on-a-chip (SOC) integration. However, the challenges to sustain such an exponential growth and to achieve such gigascale integration have shifted in a large degree from the process and manufacturing technologies to the design technologies. For example, the study by SEMATECH showed that although the level of on-chip integration, expressed in terms of the number of transistors per chip, increases at an approximate 58% annual compound growth rate, the design productivity, measured in terms of the number of transistors per person-month, grows only at a 21% annual compound rate. Such a mismatch of silicon capacity and design productivity, if not resolved timely, will seriously limit the potential of achieving high-degree on-chip integration. Therefore, a great deal of innovation in design and test technologies is needed in order to extend Moore’s Law into the next two decades.

This project plans to investigate and develop innovative design and test methodologies, tools, and algorithms to enable efficient giga-scale SOC integration in nanometer technologies. SOC designs are highly complex, not only in terms of the high transistor count, but also in terms of large numbers of heterogeneous components and technologies to be integrated on a single chip. A giga-scale SOC may include embedded CPUs, DSPs, FPGAs, various kinds of embedded memories, such as SRAMs, DRAMs, and FLASH memories, as well as possible multiple analog and RF components. Therefore, SOC designs require a wide range of knowledge and design experience as well as a complex set of software tools to support such heterogeneous integration throughout the entire design process. Although the promise and importance of SOC designs have been well recognized in the past few years, only limited research related to SOC designs has been reported, largely due to the fact that a single researcher or research group usually has expertise in one or a few areas related to SOC designs, and has difficulties developing a complete SOC application and comprehending the entire SOC design process. A notable exception is the Giga-Scale Silicon Research Center (GSRC), directed by Prof. Newton at UC Berkley under the support of MARCO, which involves over 25 faculty members from a wide range of research institutes. However, its funding level ($10M/year) is 20 to 50 times higher than a regular NSF award in the design automation program (in fact, higher than the total budget of the design automation program).

In order to assemble a research team of critical mass to fully comprehend various issues in SOC designs, yet stay within the funding level of NSF support, we take a novel approach and propose to establish an International Research Center on giga-scale SOC designs. The proposed Research Center involves 15 senior researchers from the U.S., Taiwan, and China. The requested funding from the National Science Foundation will be used to support researchers from the U.S. The Center is simultaneously applying funding from the National Science Council (NSC) in Taiwan and the Chinese National Science Foundation (CNSF) to support the proposed research activities by researchers from Taiwan and China, respectively. Additional funding from the NSF international program is requested to facilitate international collaboration. The participation of researchers from Taiwan and China is important to the success of the proposed research effort. All are from the best universities in Taiwan (National Tsing Hua University and National Chiao Tung University) and China (Tsinghua University and Peking University). They have many years of research experience in electronic design automation and/or circuit designs and have strong research records. Many students graduated from these institutions are now prominent researchers with outstanding contributions in the areas of semiconductor technologies and electronic design automation. In addition, the researchers from Taiwan are working on establishing a close working relationship between the Center and one or two fabrication foundries in Taiwan. This will be very beneficial to the proposed SOC research. The dominant portion of the world’s largest and most advanced integrated circuit fabrication foundries are now located in Taiwan. In the SOC design era, system integration happens at fabrication foundries during IC manufacturing, as opposed to in system houses through PCB board-level assembly, as in the past.
The proposed research activities include investigation and development of efficient SOC synthesis tools and methodologies, SOC verification, test, and diagnostic technologies, and an SOC design driver that motivates and validates various synthesis, verification, and test techniques developed during the course of our research. We plan to use an SOC design of a network processor as the design driver, which includes embedded CPUs, DPSs, FPGAs, and various kinds of memory components. The research on SOC synthesis tools and methodologies includes design specification, design partitioning, synthesis and optimization for embedded DPSs and FPGAs, physical synthesis for full-chip assembly, and synthesis techniques for design re-use. The research on verification and test focuses on functional verification, self-test using on-chip programmable logic, analog and mixed-signal self-test, and test for embedded memories. The outcome of this research project will be innovative design methodologies, tools, and algorithms that enable efficient giga-scale SOC integration in nanometer technologies in this and succeeding decades. This Research Center also provides an excellent opportunity to train the next generation of scientists and engineers inasmuch as the graduate students involved in this project will be exposed to a wide range of challenging problems, from circuit design, to system architecture, to development of new synthesis, verification, and test tools related to giga-scale SOC integration. They will have the opportunities to work with some of the best technologies and scientists in these areas across the Pacific Ocean.

The rest of Section 3 is organized as follows: Section 3.2 describes organization and task assignment of the proposed Center, and Sections 3.3 to 3.5 discuss our proposed research on design drivers, synthesis environment and methodologies, verification, test, and diagnostics. Section 3.6 discusses the plan for collaboration within the Center. Section 3.7 discusses the educational impact of this project. Finally, the results from prior NSF supports to Prof. Cong and Prof. Cheng are listed in Section 3.8.

### 3.2 Center Organization

The Center will be directed by Prof. Jason Cong from the University of California, Los Angeles and Prof. C. L. Liu from the National Tsing Hua University in Taiwan. It involves the following senior researchers (faculty members) from the U.S., Taiwan, and China.

#### Research Team by Institutions

**US**
- UCLA: Jason Cong
- UC Santa Barbara: Tim Cheng

**Taiwan**
- NCTU: Jing-Yang Jou

**China**
- Tsinghua Univ.: Jinian Bian, Xianlong Hong, Zeyi Wang, Hongxi Xue
- Peking Univ.: Xu Cheng

#### Research Team by Tasks

- Design driver (Task leader: Cheng-Wen Wu)
  - Processor: Xu Cheng
  - DSP: Youn-Long Lin
- Embedded memories: Youn-Long Lin and Cheng-Wen Wu
- Embedded FPGAs: Jason Cong

- Synthesis, Modeling, and Physical Design (Task leader: Jason Cong)
Detailed discussions concerning collaboration within the Center will be given in Section 3.6. Biographical sketches of two senior researchers from the U.S. are given in Section 5, followed by a brief biography for each senior researcher from Taiwan and China.

3.3 Design Drivers (Led by Cheng-Wen Wu, NTHU)

Because SOC design is still at its infancy, the requirements for the design technologies are not totally clear. Therefore, it is important to develop a design driver, which will be a realistic design using the SOC technology, and use it to identify detailed requirements of various design technologies and provide a necessary test case to the researchers for design tool and methodology research. Therefore, the first task of our SOC Center is to identify a design driver. We anticipate that a network processor will be chosen.

3.3.1 Application: Network Processor (NP)

Software-based routers will be phased out in the near future. In order to provide the performance required by next-generation networks, specialized network processors (NPs) are needed. Their typical functions may include one or more of the following: 1) segmentation (frame) assembly and reassembly, 2) protocol recognition and classification, 3) queuing and access control, 4) traffic shaping and engineering, and 5) quality of service. The most important factors in an NP include programmability, performance, management, and routing. First, the NP must be easily programmable in order to support customization and the rapid integration of new and existing technologies. The second requirement for NP is to support a large number of high-bandwidth connections, multiple protocols, and advanced features. Also, it should be able to provide wire-speed, non-blocking performance. Support for services such as security management and enforcement, performance and traffic-flow statistics, traffic filtering, etc., is also typically required. Finally, after identifying, classifying, and accounting for incoming traffic flows, the NP should make forwarding decisions based on pre-programmed information. Given these requirements, we shall propose an advanced NP architecture as shown in Figure 1.
The NP will contain the following cores: CPU, DSP, memories (including ROM, SRAM, DRAM, and possibly flash memory), FPGA, IO and user-defined function (UDF), etc. These cores will serve as the drivers for the technologies to be developed in this project. They are explained below.

3.3.2 Network Processor Components

3.3.2.1 CPU (Peking University: Xu Cheng)

By the end of 1999, the research group led by Prof. Cheng at Peking University has developed an infrastructure (named JBCODES) to support microprocessor design and corresponding compiler and assembler development. JBCODES includes: JBRC (retargetable compiler), JBASM (assembler generator), JBDisASM (disassembler development kit), JBISASim (trace-driven instruction-set architecture evaluation tools), JBCacheSim (cache performance evaluation tools), and JBWorkBench (programmer’s workbench). Using JBCODES, Prof. Cheng’s group has designed a 16-bit low-power embedded and compiler-friendly microprocessor core (JBCore16). The JBCore16 architecture is based on RISC principles. There are 87 instructions in its instruction set, and 3-stage pipelining is employed so that all parts of the processing and memory systems can operate continuously. Harvard architecture makes JBCore16’s pipeline more efficient. JBCore16’s high code density and low-power design can satisfy the requirements of embedded systems. In addition, JBCore16 supports multiple modes of operation: user, supervisor, interrupt, fast-interrupt, and user-defined instruction. A prototype of JBCore16 was implemented on an Altera Flex FPGA, and all C programs of SPEC-92 can run efficiently on the prototype board at 20 MHz clock frequency.

A 32-bit ARM-like embedded microprocessor, named JBCore32, is being developed and will be used in this project. JBCore32 supports both the 32-bit instructions set and a corresponding compressed 16-bit instruction set, allowing the user to trade off between high performance and high code density. JBCore32 is implemented using 5-stage pipelining consisting of instruction fetch, decode, execution, memory access and write-back stages. The JBCore32 has on-chip instruction and data caches. In addition, its MMU functions could support a full demand-paged virtual memory operating system and real-time embedded operating systems. In order to make the instruction pipeline running with least structural hazards, multiple functional units are provided. The JBCORE32 is expected to run all C programs in

![Network Processor Architecture](image-url)
SPEC-95 efficiently. To satisfy SOC requirements, JBCore32’s on-chip bus architecture will support peripheral design reuse and efficient production test.

The proposed network processor will include not only a high-performance CPU, but also some protocol engines and special-purpose processors. This will lead further refinement of JBCore32’s architecture to meet the NP application. We believe a CPU that integrates a multiple-issue super-scalar RISC with necessary hardware support for protocol processing, together with the help from a DSP, will be a good solution for NP.

3.3.2.2 DSP (NTHU, Youn-Long Lin)

Among all IPs, embedded processors are among the most important. For network applications, embeddable DSP core is a must. An advanced DSP core is being developed at the National Tsing Hua University (NTHU). Since the target application is networking, we shall first analyze the characteristics of such an application. The design of the instruction set will emphasize code density, power consumption, performance, and compiler friendliness. The implementation will be synthesizable RTL in Verilog HDL. We shall target it for a 0.18-0.15um CMOS low-power library. Our goal is 1GOPS at no more than 500mW.

In the first year, we shall focus on ISA design and FPGA prototyping: 1) collect and analyze application programs in networking and communication; 2) study the characteristics of other DSP and embedded RISC including TI, ADI, Lucent, Motorola, 3DSP, ZDSP, DSP-G, BOPS, ARM, MIPS, Tensilica and ARC; 3) define the ISA with adequate consideration of code density and parallelism; 4) evaluate datapath options including multiple MAC units, on-chip memory, address generation units, SIMD support, zero loop overhead, arithmetic saturation, power management, etc.; 5) implement the DSP using Verilog HDL and FPGA. In the subsequent years, we shall focus on test chip implementation and system integration.

3.3.2.3 Embedded Memories (NTHU/GUC: Cheng-Wen Wu and Youn-Long Lin)

Embedded memories are the most popular cores in SOC applications. Specifically, embedded ROM and SRAM cores have been widely used in the industry, and embedded flash memory cores are finding more and more applications. As for embedded DRAM (eDRAM), it provides high-capacity storage at a higher data rate as compared with commodity DRAM whose data rate is limited by the number of pins available. Also, eDRAM reduces overall power consumption and hardware cost. As we enter the deep submicron age and continue to shrink the feature size, we shall find chips to be more and more pad-limited. The proposed NP without eDRAM will be such a case. Therefore, merging DRAM and logic is expected to benefit the system IC industry. In fact, the merge has begun to appear in various ASIC and microprocessor designs and advanced computer architectures. Of course there are challenges in merging DRAM and logic, such as process optimization for the combined DRAM and logic, and novel design and test methodologies for guaranteeing its performance, quality, and reliability. Testing the eDRAM is more difficult than testing the commodity DRAM. The first test issue is accessibility. Accessing the DRAM core from an external memory tester is costly when the DRAM core is embedded in a chip and surrounded by logic blocks. Proper design-for-testability (DFT) methodology must be provided for core isolation and tester access, and a price has to be paid for the hardware overhead, performance penalty, and noise and parasitic effects. Even if this is manageable, memory testers for full qualification and testing of the eDRAM will be much more expensive due to increased speed and I/O data width, and if we also consider engineering change, the overall investment will be even higher. A promising solution to this dilemma is built-in self-test (BIST). With BIST, the tester requirement for eDRAM can be minimized, and the memory tester time can be greatly reduced throughout the entire test flow of the eDRAM. Also, the total test time can be reduced since parallel testing at the memory bank as well as the chip levels is easier. We shall also investigate the built-in self-repair technology to further eliminate the requirement of laser repair for the DRAM core.

We shall investigate all necessary test, diagnosis, and repair technologies for embedded memories, including ROM, SRAM, DRAM, and flash memory. The details will be described later in the section on verification and test (Section 3.5). We shall also seek the collaboration of Global UniChip Corp. (GUC) to provide their memory cores for integration into the NP chip.

3.3.2.4 Embedded FPGAs (UCLA: Jason Cong)

Many research results and industrial forecasts have concluded that future SOC products will include embedded microprocessors, embedded memories, and customized ASICs, as well as a significant portion of embedded FPGAs. Since the design complexity is much higher and the design cycle is considerably longer for giga-scale SOC designs, having embedded FPGAs in a SOC solution enables the use of one product to serve multiple applications and continuous adaptation of the product to the evolving interfaces and standards without going through the lengthy re-
design process. This will considerably reduce the time-to-market and design cost. Moreover, since the mask cost has increased sharply for nanometer designs, field-programmable SOCs (FPSOCs) will significantly reduce the manufacturing cost, as it can be easily adapted to multiple applications and/or design changes without going through re-fabrication. Furthermore, FPSOC provides a solution with much higher performance and smaller area and power dissipation compared to an all-software implementation using microprocessors. We plan to use the embedded FPGA in this NP design driver and provide customized circuitry to support various kinds of routing protocols and network functions (such as various priority schemes, data compression and decompression algorithms, encryption and decryption algorithms) so that a single SOC implementation of the NP design can be reconfigured for different network environments and performance/bandwidth/power requirements.

We shall investigate several possible approaches for developing embedded FPGAs in SOC. One approach is to develop a module generator for embedded FPGAs to be used in our SOC prototype implementation. In particular, we plan to investigate the possibility of using the novel FPGA architecture recently developed at UCLA, which is based on k-input single-output PLA-like cells, or, k/m-macrocells. Each cell in this architecture can implement a single output function of up to k inputs and up to m product terms. Our study shows that a k/m-macrocell with only a relatively small number of product terms (m < k+3) is practically equivalent to a k-LUT (lookup-table) in terms of functional implementation capabilities. As a result, we can afford to use k/m-macrocells with large k as basic programmable cells, which significantly reduces the level of the circuit (and the interconnects associated with each level) and achieves better circuit performance. Note that it is not feasible to use large k-LUTs to reduce the circuit depth, as the area of a k-LUT grows exponentially with respect to k while the area of a k/m-macrocell grows only at a quadratic rate under the assumption that m is linearly related to k. Our experimental result indeed shows k/m-macrocell based FPGAs can outperform 4-LUT based FPGAs in terms of both delay and area after placement and routing. We have developed near-optimal depth-mapping algorithms for the k/m-macrocell based FPGA architecture [3].

The other alternative to developing a new embedded FPGA architecture is to license an existing FPGA architecture from one of the FPGA vendors and include it in our SOC prototype. UCLA has established excellent working relationship with almost all major FPGA vendors, including Actel, Altera, Lucent Technologies, and Xilinx. They have been supporting the FPGA-related research in the past 5 to 10 years under the California MICRO Program. The RASP FPGA synthesis system RASP[4] developed at UCLA can be targeted to most of the architectures from these FPGA vendors, and many algorithms in the RASP system have been adopted in the commercial synthesis systems developed by these vendors. Most of these companies have showed a strong interest to explore the FPSOC technology as part of their future product roadmap. We plan to form partnerships with these companies once the proposed International Research Center is funded by NSF.

3.3.2.5 Target Technology

The target technology is 0.15um CMOS, or any advanced and mature technology that will be available early in 2003. An industry partner in Taiwan will be sought for fabricating the NP test chip.

3.4 Synthesis Environment/Methodology (Led by Prof. Jason Cong, UCLA)

Developing an automatic synthesis environment and methodology for giga-scale SOC designs is a highly complex and challenging task. Using the design driver described in Section 3.3, we shall explore a number of important research topics related to SOC designs, including design specification, design partitioning, reargetable compiler for embedded processors, synthesis and optimization techniques for DSPs, synthesis and technology mapping for embedded FPGAs, and a set of issues related to embedded ASIC designs. These tasks are inter-related and form an exploratory SOC design environment as shown in Figure 2. The remainder of this section discusses each topic and the proposed research in more detail. Note that for ASIC synthesis, we focus only on interconnect-driven high-level synthesis, synthesis for IP re-use, and physical synthesis for full-chip assembly. We assume that the remaining steps for designing ASIC components can be accomplished by off-the-shelf commercial tools (such as those provided by established EDA vendors like Synposys, Cadence, and Avant! or emerging EDA companies such as Magma and Monterey Design).
3.4.1 Design Specification (Tsinghua Univ., Jinian Bian and Hongxi Xue)

An SOC can implement a complete system including processors, memory, control circuits, programmable logic, and even analog and mixed signal circuits on a single chip. Given the complexity of SOC designs, the designer needs efficient ways to specify the system-level design and a convenient design environment to help develop SOC chips. This project plans to provide such a hardware and software co-specification and co-design environment for SOC.

Several co-design systems or tools have been developed in recent years, such as Polis [17] and Ptolemy [33][34](UC Berkeley), COSIMA[10][11](Aachen University of Technology), COSMOS[32](TIMA), IESAQ[35](University of California, Irvine), etc. Some of them use standard C or extended C to describe systems; some of them use special languages such as Esterel; while SLS of TIMA uses multi-languages to describe the individual modules. The key issue with such co-design environments is the correspondence between the presentations used in the initial specification and the function provided by the target model (virtual prototype). For instance, the mapping of the system specification language, including high-level concepts such as distributed control and abstract communication, onto low-level languages such as C and VHDL is a non-trivial task [7][16]. In order to reduce the gap between the specification model and the virtual prototype, several co-design environments start with a low-level specification model. COSIMA starts with a C-like model called Cx [10][11]. VULCAN starts with another C-like language called hardware C. Several co-design tools start with VHDL [30]. Only a few tools tried to start from a high-level model. These include Polis [17] that...
starts with an Esterel model [6][5], Spec-syn [8][9] that starts from SpecCharts, and the work reported in [18][25][26] that starts from LOTOS [12].

In this task, we propose to develop an integrated hardware/software co-design environment for SOC. It includes a multi-language system description using C and VHDL, with C-VHDL co-simulation and co-verification. We shall also develop a tool to transform a C description for hardware components to a VHDL description, in order to apply automatic synthesis for it later on. Our research will include the following tasks.

1. C-VHDL multi-language specification: In multi-language specification, one can use different languages (C, C++, or VHDL) for different modules. It allows the user to describe a system using a combination of C or VHDL. The software modules are described in C or C++ in general, while the hardware modules can be described in both C and VHDL. In this approach, the key challenges are multi-language co-verification and interface synthesis. We will research how a module is described in C.

2. C to VHDL transformation: After HW/SW partitioning, the C description of hardware parts will be transformed to a VHDL description. The key problem is to find the corresponding relationship between C and VHDL. We shall analyze how the functions of C can run in parallel and how to transform them to corresponding processes of VHDL. We should also study how to determine the length of each variable in VHDL.

3. C-VHDL co-simulation: We have already developed a VHDL simulator prototype which transforms VHDL to C++ and runs the C++ program to realize the simulation. We only need to merge the transformed C++ programs and C specification as one executable program to realize co-simulation. The key problem is to determine how they interact and communicate with each other.

4. C-VHDL co-verification: We have been working since 1996 on formal verification for VHDL synchronous design using a model-checking technique. We shall expand it to handle C-VHDL heterogeneous specification. Finite State Machine will be extracted from the C description. Then, we can apply the existing approach to verify it. In order to cope with complex relationship between various modules, we plan to use a parallel-hierarchical FSM model to represent the system. We shall study the efficient methods for reachability analysis and verification under this model.

The synthesis group at Tsinghua University (Beijing, China) has done extensive research on logical- and high-level design automation tools since the 1970s. In the early years, we developed logic-functional-switch mixed-level simulators and researched logic-level and high-level synthesis. In the 1990s, we developed a set of VHDL-based design and synthesis tools, including VHDL compiler, simulator, visual VHDL entry tool, and graphical debugger. Since 1996, we have done much research on formal verification. We developed an equivalence verification tool using BDDs for combinational logic circuit and FSM models, as well as verification methods for synchronous VHDL design. The focus of our research is to overcome the high complexity associated with the verification problem. Another ongoing research project currently in our group is merging layout-driven logic synthesis with layout, including a timing-constraint multi-level logic synthesizer based on BDD and a local re-synthesizer for timing constraint after placement. These extensive research experiences will enable us to successfully carry out proposed tasks. Our group will also be working on interconnect-driven high-level synthesis as described in Section 3.4.3.

### 3.4.2 Design Partitioning (NTHU, Allen Wu)

SOC-based systems are usually implemented with mixed hardware and software components. The functionality of a system can be realized either as software components running on a processor core or application-specific hardware components. Translating a system specification into a target system architecture is referred to as the hardware/software partitioning problem. Since system-design specification is done using mixed the C and VHDL languages (as described in Section 3.4.1), in this research, we shall study how to convert the C-VHDL system specification into the target SOC architecture. We shall study the following two topics:

1. In order to support system partitioning design decisions, we need to develop a series of C-VHDL-based design estimation and exploration techniques. We shall develop cost/performance estimation methods from the C-VHDL-based system specification. Based on the estimation methods, we shall develop design exploration techniques by trading-off hardware/software implementation of different parts of the system.

2. We shall develop algorithms/methods to partition the C-VHDL-based system specification into hardware/software subsystems. If we decide to implement part of the C specification using a hardware approach, we shall use the C to
VHDL transformation method (developed in the research of Section 3.4.1) to convert the C specification into a VHDL-based hardware specification. Finally, we shall use the C-VHDL co-simulation and co-verification methods (section 3.4.1) to verify the partitioning result.

3.4.3 Interconnect-Driven High-Level Synthesis (Tinghua Univ., Jinian Bian and Hongxi Xue)

As the feature size of the integrated circuits is down to deep sub-micron, or even nanometer technologies, traditional methods for high-level synthesis without considering the effect of interconnections are no longer able to meet the high-performance requirement as interconnect delay becomes the dominating factor in determining the system performance. In this project, we propose research and development of an interconnection-oriented high-level synthesis tool.

The need for new, efficient high-level synthesis techniques is very strong, especially in the SOC era, for the following reasons:

1. Systems are complex: They can no longer be specified manually at a lower level, such as gate-level and RT-level, where clock cycles need to be detailed. Higher-level abstraction models are required to master the complexity.

2. Systems are heterogeneous: New specification and design methods are needed to handle the cases where different languages and design style may be used within the same design.

3. Complex architectures are required to implement future electronic systems: These may include several processors organized around a hierarchical bus structure using a distributed memory structure. A new generation of system design methods allowing the integration of heterogeneous components is required.

4. Interconnection delay must be considered in high-level synthesis to achieve high performance. The outcome of high-level synthesis defines the internal wires in various resources and interconnection wires among the resources. Therefore, wire generation and optimization should be emphasized in the high-level synthesis.

In order to estimate the interconnection information and to reduce the effect of interconnection wires, several studies combined high-level synthesis with floorplanning so that physical information is considered in the process of high-level synthesis [36][37][38][40][41][42][45][46][48]. The key problem is to find efficient algorithms to handle the complexity of the combined problem. In general, there are two kinds of approaches: (1) constructive approaches, which carry out synthesis and floorplanning simultaneously, such as the 3D-algorithm [49] and the GB algorithm [6]; (2) iterative approaches, which combine high-level synthesis with floorplanning by iterating between scheduling, allocation and floorplanning in order to achieve the target clock rate [37][38]. However, the existing constructive algorithms are lack of consideration of the global design information, while the iterative approaches have high complexity and consume too much time.

In this project, our goal is to find an efficient method to provide tradeoff between the two approaches. A key emphasis is to reduce the impact of global interconnects on circuit performance. We shall consider the two approaches simultaneously. We plan to study the interaction between synthesis and floorplanning, and to find an efficient flow. In particular, we plan to study how to model the global interconnects during scheduling and allocation, and analyze the impact of interconnect delays on circuit performance.

Our high-level synthesizer will accept the C/VHDL behavior description described in Section 3.4.1. We shall develop an internal representation which is able to represent both a hierarchy of CDFGs with timing constraints and the geometric information obtained from floorplanning.

We shall combine floorplanning techniques with high-level synthesis. Based the internal representation, the design task is partitioned to a set of functional-units and then floorplanned. The objective function includes not only the total cost of the functional-units, but also the number and the length of interconnection wires.

In the phases of scheduling and allocation, the behavioral and physical domains will be unified to generate the placement information for each component introduced in scheduling and resource allocation. The result must meet the timing constraints. It is important that the interconnection delays in the data path components are calculated during the phase. By iterating and refining scheduling, allocation and floorplanning, we can gradually converge to a clock rate that satisfies the timing constraints, not only during high-level synthesis, but also after the final layout.

Finally, interconnect optimization is needed. It is important to analyze the interconnect wires between the controller and data path components, and to minimize their delays. These interconnects are usually longer and have great impact
on the overall performance. Techniques such as buffer insertion, wire sizing and spacing, as well as re-timing over global interconnects will be considered. This part will be done jointly with Prof. Cong’s research group at UCLA.

3.4.4 Retargetable Compiler Infrastructure and Assembler’s Generator (Peking Univ., Cheng Xu)

The design of a modern microprocessor needs to consider tradeoffs among software technology, system architecture and micro-electronic implementation. Evaluating the microprocessor’s performance during this procedure is one of the primary tasks of the simulation environment support for microprocessor designs. It is important for the compiler (assembler) developer to be able to implement corresponding compilers for target machines with decreased cost and shortened time-to-market, while making full use of the characteristics of the new machines, in order to make more accurate and efficient performance simulation and evaluation.

As an important part of compiler infrastructure, a retargetable compiler(assembler) can be easily retargeted to a new machine architecture, including the new instruction set, as well as other new features.

The main difficulty in developing the retargetable compiler is to effectively describe machine features such as the pipeline, and to generate a corresponding compiler based on this machine definition efficiently, with good optimization.

The NCI( National Compiler Infrastructure) [http://www.cs.virginia.edu/nci/] project aims to develop a common compiler platform to support the collaboration of compiler researchers and to facilitate transfer of technology to industry. NCI builds a complete and convenient compiler-developing platform to facilitate the development of the compilers. The toolkit includes the CSDL (system description language), ASDL (Abstract Syntax Description Language), VPO (very portable optimizer), and so on. The compiler of LCC, a retargetable compiler developed at Princeton University, can be retargeted to a new machine using the MD file which describes the features of the machine.

In the JBRC (Jade Bird Retargetable Compiler) system developed at Peking University, we first take the abstract syntax tree as an intermediate representation, which is target-independent. This leads to the well-defined structure of our compiler, whose code generator with encapsulated machine-dependent code and data is clearly separated from the front end. Second, we use a code-generator to produce the instruction selector automatically from a compact specification for a specific target machine. This simplifies the work of retargeting JBRC to a new machine. We use the method of BURG (bottom-up rewrite system) [50] in our system to finish instruction selection. But there are some insufficiencies currently in the JBRC system: there is little optimization in the backend, and the C language set we supported is not complete.

At present, we are involved in the research of a compiler optimizer, especially in the portable and configurable optimizer oriented to the machine feature, such as pipeline and VLIW and other machine resources. At the same time, we are improving the robustness of the front-end to support the complete ANSI C instruction set, aiming at passing all of C programs in SPEC95 benchmarks. We shall redefine the intermediate representation in the next step to separate the front-end more efficiently in order to add some optimization to the front-end.

There are two challenges in designing an assembler generator: The first is to distinguish different rules which can be used to map assemble language to binary code by all appearances. We should design a specification language to describe the rule. The second is to generate an assembler that can generate efficient codes for special microprocessors.

The New Jersey Machine-Code Toolkit has made good progress along this line [51][52]. SLED(a Specification Language for Encoding and Decoding) is the specification language in their project and is included as part of the NCI-VPO project. This is an excellent project, but the SLED is complex and huge.

We have developed a specification language for encoding, which describes abstract, binary, and assembly-language representations of machine instructions and partial structures of microprocessors including registers, memories and others. Guided by a JBASM-SL specification, JBASM generates an assembler automatically. Programmers can write such specification at an assembly-language level of abstraction. After analysis JBASM recognizes the rule and has the ability to generate the binary representations used by the hardware. JBASM-SL is suitable for describing both CISC and RISC machines. We have specified representations of MIPS R3000, SPARC, Alpha, Intel 8086 instructions, as well as for our new processor, JBCore16. JBASM-SL uses four elements: fields and tokens describe parts of instructions; opcode describes binary representations of instructions or groups of instructions; addresses and
constructors map between the abstract and binary levels. In addition, SL can also describe macro- or pseudo-instruction and some data directions.

Efficiency is another goal in our project. We use technologies to increase the speed of assembling (such as efficient hash algorithms and build-in linker). JBASM also provides interfaces that the user can use to program special functions for special rules.

With retargetable ability, however, JBASM’s assembling speed is slower than a custom-made assembler. It is mainly due to the lack of optimizer for specification instructions. This is an area that needs improvement.

The main objective in the coming year is to extend the JBASM-SL to describe the OBJ file format, so we can separate assembler and linker. Having a retargetable linker, we can increase the speed of translation and reduce the workload of programming an integrity assembler. On the other hand, we should design how to describe the optimization algorithm taking place in the assembling process. How to define the specification language concisely and completely is the focus.

We plan to improve the compiler’s optimization strategies, both at machine-independent and machine-dependent levels, and redesign the assembler generator to create a hardcode assembler more efficiently once the proposed International Research Center is approved by NSF.

3.4.5 Synthesis and Optimization for DSP Cores (NTHU, Tingting Hwang and J.K. Lee)

The design of DSP cores will emphasize code density, power consumption, performance, and compiler friendliness. For related CAD technologies, we shall focus on technologies for low power design. The results of our studies will be used to design the Instruction Set Architecture (ISA) of the DSP processor. For the compiler friendliness, we shall study the instruction set description language for retargetability and DSP library porting.

3.4.5.1 Low-Power Design Technology for DSP Cores

Lower power design can be carried out at architecture design, logic design, and physical design levels. In this proposal, we shall study low-power design issues in the context of programmable DSP core at the architecture design level. The following topics will be studied:

(1) Design of Power Management Instruction: One effective way to reduce power consumption in a circuit is to turn off subcircuits that are inactive during certain machine cycles. To this end, we need to partition a circuit into parts so that different parts can be turned off by the control logic. For a programmable DSP core, we shall study component architectures that allow dynamic circuit partitioning. For such “partitionable” architectures, we shall study and develop their corresponding power management instructions.

(2) Design of Low Power Controller: In signal and image processing, cyclic execution of a few instructions is often the dominant part of a program, because these applications often involve computations built around convolutions, transforms, and other matrix computations. However, the controller of a general-purpose DSP is designed to decode all instructions all at once. We shall study the concept of "coupled controllers." For a coupled controller, only one of the sub-controllers will be activated most of the time, which can, consequently, lead to substantial savings in power consumption.

(3) Synthesis of High-Performance and Low-Power MAC: MAC (Multiply and Accumulate) is one of the most important operations in a DSP. We shall study the problem of synthesizing high-performance and low-power MAC modules.

(4) Low-Power High-Performance Compiler Optimization Technologies: We shall develop a set of compiler optimization technologies with DSP/CPU features to focus on low-power computing without performance penalty. Those technologies will try to reduce DSP/CPU components’ activities, voltage transitions on data/instruction bus, etc.

3.4.5.2 Instruction-Level Simulator Generator

A cycle-correct instruction-level (IL) simulator is the first element of the tool chain for a new CPU design. Any behavior pattern’s mismatch between the IL simulator and the real processor may cause unpredictable software bugs. The characteristics of our simulator generator are described below.
(1) RTL/JBASM-SL Based Instruction Level Simulator Generator: The IL simulator generator will understand RTL/JBASM-SL (mentioned earlier in section 3.4.4) to get hardware profiles from target’s RTL information and JBASM-SL descriptions to produce a cycle-correct IL simulator.

(2) Common Information Grapping Interface: The series of generated IL simulators will be promised with compatible profiling interfaces. With this common interface, the collections/analysis tools can be used on CPU/DSP simulators of the next series.

(3) Common Data Modifying Interface: The series of generated IL simulators will be promised with the capability for run-time instruction/memory/register modification. With this capability, run-time optimization with a variety of issues can be loaded with different sequences to evaluate resource benefits.

3.4.5.3 DSP Library Porting

(1) ISDL/Hardware Description Language-Based DSP Library Design: We propose to design a high-performance library based on DSP-understanding compiler derivatives. A compiler with such features can extract information from hardware architecture profiles to generate more efficient machine codes.

(2) Virtual Machine-Based DSP Library Design: We propose to design an environment that hides the details of the underlying real DSP architecture from the designer/programmer. This approach enables developers to write code in an ideal full feature DSP environment. The compiler will fill the missing features between the target architecture and the virtual DSP environment with predefined and efficient subroutines.

3.4.6 Synthesis and Technology Mapping for Embedded FPGAs (UCLA, Jason Cong)

Much progress has been made on FPGA synthesis and technology mapping in the past decade. For example, the RASP synthesis system for SRAM-based FPGAs developed at UCLA ([53]) includes many advanced FPGA synthesis algorithms, such as depth-optimal mapping (FlowMap [54]), duplication-free area-optimal mapping (DF-Map [55]), mapping with resynthesis (FlowSYN [56]), simultaneous mapping with optimal retiming (TurboMap [57]), and so on, for generating highly optimized lookup-table (LUT) based netlists. It also includes a set of architecture-specific technology mapping routines to map a generic LUT network to a network of programmable logic blocks (PLBs) of various SRAM-based FPGA architectures, including those with a cluster of LUTs, an array of heterogeneous LUTs, or an array of uniform LUTs with embedded memories (such as Flex 10K devices from Altera). The focus of this research, however, is on fast incremental synthesis for FPGAs. Including embedded FPGAs in an SOC provides a convenient way to accommodate design changes and support design iterations (so that design changes can be made in a very similar way to software development). As much as we strive for fast design convergence, design iteration is unavoidable due to the ever-increasing design complexity and rapid changing market considerations (which often result in changes in design specifications). Efficient ways to handle minor changes in the design (such as modifications to the netlist or FSM) will be much needed. Our research will focus on the following two directions:

Efficient incremental synthesis techniques: First, we shall develop a set of efficient synthesis algorithms to handle various incremental changes so that we can satisfy various design constraints while making minimal perturbation to the original synthesis solution. For example, when a new state or a new transition edge is added to an FSM, we need to come up with a new state encoding solution so that the resulting Boolean network is close to the original one, yet meets the area and delay constraints. Existing incremental synthesis techniques are based on local restructuring, such as adding/removing redundancy, reconnecting wires based on internal symmetries, or re-synthesizing nodes and wires using SPFDs. These techniques have been limited to combinational circuits and used in the past on an adhoc basis. They need to be studied more systematically, not only in the context of combinational circuits, but also for sequential circuits, with consideration of the rich flexibility provided by programmable logic elements and programmable routing architecture. We shall develop efficient algorithms for partial resynthesis for incremental netlist changes under the performance and area constraints (imposed by higher-level design tools) to achieve the following three levels of objectives for the incremental synthesis:

- **Level 1.** No change in the topology of the mapped programmable logic block (PLB) netlist, and thus no change in the place-and-route solution, or

- **Level 2.** No introduction of new PLBs, but minimal changes in the interconnects, or
Level 3. Minimal changes in the technology-mapping and place-and-route solution.

The main objective is to minimize the effort of incremental place-and-route in the subsequent steps. The system automatically retargets for the next level objective (say Level 2) once it concludes that the current level objective (say Level 1) is not possible to meet. The incremental design changes in the netlist will be decomposed into a sequence of primitive change operations, such as adding or deleting a connection, adding or deleting a gate, or changing the function of a gate.

**Design for incremental synthesis:** If design iteration is unavoidable, it is important to develop a new design methodology with the objective to accommodate incremental synthesis as much as possible. For example, we shall investigate how to come up with a state encoding scheme for an FSM so that it can accommodate as many incremental changes to the FSM as possible without completely re-encoding and re-synthesizing the FSM. Similarly, given certain area slack in a design, we shall study how to distribute the set of functional blocks into a floorplan solution so that it can accommodate a maximum amount of incremental layout changes without drastically changing the floorplan topology. We need to develop metrics to quantitatively measure the ability to accommodate incremental changes and a new design methodology to optimize such a metric.

We shall first develop the theory, general techniques, and metrics to support incremental synthesis and design for incremental synthesis. Then, we shall apply our results to develop an efficient incremental synthesis tool for the target FPGA architecture as defined in Section 3.3.2.4. In particular, we shall develop an efficient incremental synthesis algorithm for the $k/m$-macrocell based FPGA architecture. Also, we plan to use such tools and algorithms to guide the $k/m$-macrocell based FPGA architecture design, so that it can easily accommodate incremental changes in the most efficient way.

### 3.4.7 Synthesis Techniques for IP-Reuse (NTHU, Allen Wu)

Due to the rapid advance of fabrication technologies, silicon capacity is doubling every 18 months. This allows companies to build more complex systems on a single chip. However, the ability to develop such complex systems in a reasonable amount of time is diminishing with the rapid increase in complexity. The gap between silicon capacity and design productivity seems to be widening at an ever increasing pace, slowing the growth of the semiconductor industry.

In order to solve the productivity gap problem, three approaches have been proposed: (1) platforms, (2) reuse and (3) synthesis. In the platform approach, semiconductor vendors provide a universal SOC platform consisting of one or more core processors and many smaller peripheral processors for handling different I/O protocols and encoding/decoding functions. In the reuse approach, it is assumed that SOC designs will be assembled from many different blocks of IP provided by a variety of sources. In the synthesis approach, the SOC chip will be synthesized from a high-level functional description and tuned for particular applications and fabrication technology.

In this research, we shall focus on the reuse approach. In the reuse approach, it is assumed that SOC designs will be assembled from many different blocks of core/IP (Intellectual Property) provided by a variety of sources. In today’s ASIC design flow, reusing RTL components is a common practice. However, reusing simple RTL components may not be adequate in alleviating the design complexity of SOC designs. In order to reduce design complexity and shorten design-cycle time, reusing complex cores becomes a necessity for SOC designs. However, reusing complex cores for a design project is not a trivial task.

In this study, we shall investigate the following topics:

1. The requirements for reusing a complex IP and how to capture the functional and performance characteristics of IP for reuse. We shall develop a complex IPs/cores capturing method and tool.
2. How to apply higher-level synthesis techniques (e.g., behavioral level) to facilitate the complex IP/core reuse process, and perform interface generation and SOC integration. We shall develop a synthesis method and tool for automatic IP reuse and system integration.
3. Develop a C-VHDL-based behavioral specification to silicon design flow. Case studies will be conducted to demonstrate the degree of productivity improvement on the proposed IP-reuse method.
3.4.8 Physical Synthesis for Full-Chip Assembly

In this project, given the limitation on resources, we are not able to include a complete research program on logic-level synthesis and physical design. We plan to use off-the-shelf commercial tools (such as those provided by either established EDA vendors like Synopsys, Cadence, and Avanti! or emerging EDA companies such as Magma and Monterey Design) for logic synthesis and physical design of ASIC components. We shall focus our research on physical synthesis for full-chip level assembly, which is a critical step in integrating heterogeneous components and technologies into a single SOC design. But this step is not well understood and there is no existing solution. Full chip level assembly is particularly important for achieving high-performance designs as the global interconnects are bottlenecks in determining system performance in deep submicron technologies. Our research in this area includes floorplanning and interconnect planning, power/ground network design, and full-chip level parasitic extraction and modeling.

3.4.8.1 Floorplanning and Interconnect Planning (Tsinghua Univ., Xianlong Hong; UCLA, Jason Cong)

Floorplanning and placement of block level is a very important part in the full-chip level assembly. Rapid increase of IC capacity makes it possible to integrate microprocessors, embedded memories, application-specific integrated circuits (ASICs), field-programmable logic arrays (FPGAs), and various analog components into a single IC. The floorplanning and block placement tool will place various modules and minimize total chip area and interconnect cost considering timing, noise, power, and specified topology/geometry constraints. Many studies have been done on floorplanning and block placement in recent years. D.F. Wong’s group proposed several algorithms to handle slicing structure by binary tree layout representation [76]. Sequence-pair (SP), BSG and O-Tree are other layout representations for non-slicing structures [77][78][79]. Based on these representations, many methods have been developed for floorplanning and block placement, which can consider various topology constraints, such as boundary constraints, abutment constraints and fixed block constraints. But there are few studies considering timing, noise and power constraints. The physical design research group at Tsinghua University has been working in this area for several years. We have proposed a new topological representation, corner block list for non-slicing floorplan, which has O(n) complexity [85]. Based on the corner block list and other representation, we have proposed several algorithms in floorplanning and placement with boundary constraints, and fixed block constraints with L/T-shape blocks [80][81][82][83][84].

As the IC technology moves to nanometer dimension and gigahertz frequencies, interconnects play the dominating role in determining the performance, power, reliability, and cost of the system. Therefore, it is necessary to consider interconnect estimation and planning at every design level. Physical-level interconnect planning is to find the best interconnect topology, wire ordering and width, wire spacing, layer assignment, etc., for all global and semi-global interconnects to meet the required performance. Prof. Cong’s group at UCLA has done an extensive and in-depth study on the design and optimization of high-speed VLSI interconnects in deep submicron designs, and achieved many interesting and original results, including interconnect topology optimization with buffer insertion [59][60][62], optimal wire sizing and spacing [62], high-speed clock net routing [64], novel approaches to interconnect performance estimation and design planning [65], interconnect-centric design flow [66], and so on.

Our proposed research on floorplanning and interconnect planning for full-chip assembly includes:

1. Improve corner block list layout representation and speed up floorplanning and placement.
2. Handle multiple constraints, such as boundary, abutment, fixed block, L/T-shape constraints simultaneously.
3. Consider timing, noise and power constraints, and buffer positions inserted by clock net synthesis.
4. Consider the effect of parasitic inductance in interconnects to improve and extend research results of design and optimization of high-speed VLSI interconnects.
5. Consider interconnect planning in floorplanning and interconnect planning driven floorplanning.
6. Incorporate the recent research results from UCLA on interconnect planning into the floorplanning package, including those on interconnect performance estimation (IPEM), wire width planning, buffer block planning, etc.

3.4.8.2 P/G Network Design (Tsinghua Univ., Xianlong Hong)

With the advance of deep submicron IC technologies, power supply design is becoming an important problem because it affects the performance of circuits considerably. There are two important problems in power/ground network design:
undesirable wear-out of metal wiring caused by electromigration, and narrowing margins caused by voltage drops. Power/ground network synthesis finds a topology for a power/ground network, and then minimizes the wiring area of the power/ground network under voltage drop and current density constraints.

Several studies on power/ground network optimization have been proposed. The method in [67] is based on feasible direction method, which may bring about the problem of zigzagging [68] which leads to poor convergence [69]. Augmented Lagrangian Function method was proposed by [70]. To avoid computation of a currents partial differential subject to conducts or resistance, both currents and conducts are used as variables and Kirchhoff’s law is used to generate loop constraints, which may result in redundant searching space and increase of the problem scale in the Augmented Lagrangian Function method. In 1999, Tan and Shi proposed an interesting algorithm [71]. The basic idea is to transform a constrained nonlinear programming problem into a sequence of linear programs. Like Mitsuhashi’s algorithm, voltages and currents are also used as variables. However, all the methods discussed above have been tested only on several small test cases. Even the biggest one [71] has only 10,000 nodes. The running time yet is quite long.

Tsinghua University has been working on power/ground network synthesis for more than three years and proposed several efficient algorithms for the design and optimization of tree-based topology for BBL (building block layout) mode and mesh-based topology for standard cell mode [72][73][74][75]. We plan to work on the improvement of optimization algorithm for mesh-based topology and developing a power/ground synthesis tool. Specific tasks include:

(1) Improve the optimization algorithm based on mathematical programming using conjugate gradient method, circuit sensitivity analysis and equivalent network.

(2) Develop a power/ground synthesis tool, which can handle tree based and mesh based topology of power/ground network.

(3) Consider Delta-I noise by parasitic inductance, multi-pad/multi-tree, movable pads.

3.4.8.3 Parasitic Extraction and Modeling (Tsinghua Univ., Zeyi Wang)

In deep submicron IC designs, we see the use of very complicated geometry and shape of the interconnect wires, and very high clock frequency (multi-giga hertz). These features lead to the strong proximity effect and skin effect in interconnects [86]. The National Technology Roadmap for Semiconductor shows that in ten years the characteristic dimension will shrink to about 70 nm, clock frequency will achieve 2.5 GH, and the number of interconnect layers will be around nine. At that time, compared with parasitic capacitance, the effect of the parasitic resistance and inductance will affect the performance of VLSI circuits in a more significant way. Even now, accurate and efficient extraction of the frequency-dependent resistance and inductance has found many significant applications, such as the clock distribution analysis [20][15], non-ideal semiconductor substrate analysis [15], interconnect analysis in packaging, massively coupled interconnect problems in RF circuits [15], and so on.

In the 1990s, many advanced numerical algorithms, such as the MultiPole Accelerated algorithm (MPA) [18], hierarchical computation [24] and parallel MPA computation [28], etc., were proposed for capacitance extraction. At the same time, many capacitance extraction tools with good accuracy and reasonable runtime were developed and commercialized by EDA vendors. Compared to capacitance extraction, the study of resistance and inductance extraction [31][27] was not very active. Currently, there are two kinds of inductance extraction methods: the volume element method [22][15] and the boundary element method [23]. The well-known extraction tool, FastHenry, developed by Kamon et al, was based on the volume element method [14]. Compared with the volume element method, the boundary element method has several advantages, such as fewer discrete variables, more accurate model and etc. Hence it has received much attention [15][23].

In the coming 5 to 10 years, because of requirements in the design of high-performance SOC circuits, in addition to the parasitic capacitance extraction, it will be very important to extract 3D interconnect inductance and resistance for interconnects with complicated geometry and under 1-4GHz of operating frequency. At the same time, due to higher frequency and more complicated 3D geometry, it is necessary to find more accurate mathematical-physical models that consider the eddy current in addition to the skin and proximity effects and develop more advanced algorithms with higher computational accuracy and speed. The proposed research work on parasitic inductance extraction includes:

(1) Determine mathematical-physical model of inductance extraction considering eddy current and skin effect.

(2) Study the relevant advanced algorithms including fast-solving method for linear equation systems.

(3) Develop a prototype of the inductance extraction tool.
Since 1990, our group has been engaged in algorithm study and software development for 2/3-D parasitic interconnect resistance, capacitance and inductance extraction. During the past ten years, about 60 papers were published, including 3 papers in IEEE Trans. on CAD. In addition, a capacitance extraction software B3D developed by our group and commercialized by Synopsys Inc. is now available in international market since last year. Compared with the widely used extraction software RAPHAEL developed by TMA (now part of Avant! Corporation), B3D can run several thousand times faster for some complex cases under comparable accuracy. These achievements indicate that our group is well qualified and positioned for the proposed research on inductance modeling and extraction.

3.5 Verification, Test, and Diagnosis (Led by Prof. Tim Cheng, UCSB)

We propose major research efforts in functional verification, test and diagnosis. For functional verification, research will be conducted in two areas: (1) Automatic vector generation and assertion checking for HDL, and (2) formal verification based on the Extended Finite State Machine model. In the test and diagnosis domain, we propose to conduct research in a number of topics. Overall, our objective is to develop test and diagnosis techniques to achieve an ultimate goal of “testless” testing and diagnosis capabilities. Specifically, we shall investigate the following topics: (1) self-test using on-chip programmable components in SOCs, (2) self-test for analog and mixed-signal components, and (3) test techniques for deep-submicron embedded memories. The Figure 3 highlights the scope, goals and directions of our research in verification, test and diagnosis.

3.5.1 Functional Verification (UCSB, Tim Cheng; NTHU, Shi-Yu Huang and Cheng-Wen Wu)

We propose to conduct fundamental research for developing an efficient engine for the applications of functional verification. Specifically, we shall investigate the following topics: (1) developing a constraint solver, employing the word-level ATPG and modular arithmetic techniques, for the application of property checking and automatic functional vector generation from HDL, (2) combining the FSM extraction and symbolic techniques for functional vector
generation, and (3) investigating the state enumeration techniques using the Extended Finite State Machine (EFSM) model.

3.5.1.1 Constraint-Solving for Functional Verification

We propose to develop a new constraint-solving engine for property checking and automatic generation of design verification vectors. The objective is to achieve a more than 10X increase in capacity for model checking and vector generation.

The current model checkers are not quite scalable to larger designs. The source of the limitations is primarily in the underlying constraint-solving engine that is the main target of this research. The proposed constraint-solving approach combines structural, word-level automatic test pattern generation (ATPG) and modular arithmetic techniques to solve the constraints imposed by the target property or target coverage metrics. This approach utilizes the strengths of both techniques in solving different kinds of constraints in the circuit and integrates them closely in a unified engine. The word-level ATPG and word-level logic implication techniques primarily solve the constraints imposed by the control logic. They also propagate the logic implications of the assignments made in control logic to the datapath. The new arithmetic constraint solver, based on a modular number system, is then employed to solve the remaining constraints in the datapath. After the initial engine is implemented and thoroughly characterized, we shall then further investigate how to closely integrate BDD and SAT techniques into the engine to further improve the performance of constraint solving.

Constraints on the datapath can be divided into two types: linear and nonlinear. We have developed a linear constraint solver based on a modular number system [98]. The linear constraint solver is highly efficient, and finds all solutions and expresses them in a closed form under the modular number system in the complexity of $O(n^3)$, where $n$ is the number of input variables. For nonlinear arithmetic constraints, derived from multipliers and shifters, we are exploring some analytical approaches like prime number factoring to heuristically enumerate the possible solutions and substitute them into the arithmetic equations so that the constraints become linear and can be solved by the linear constraint solver.

There are several potential advantages of using structural word-level ATPG and modular arithmetic, instead of satisfiability-based (SAT) [99] and linear programming techniques [100] for constraint solving: (1) We can fully utilize the high-level RTL information and perform word-level implication on both Boolean and arithmetic gates. Several techniques used to translate the implications between Boolean and arithmetic gates have been developed such that conflicting implications can be detected early; (2) Because the signal values in circuit netlist (RTL netlist) are finite-width bit-vectors, solving arithmetic constraints in a modular, instead of a general integral number system, will not miss the solutions that come from the modulation and therefore can avoid the false negative effect in generating counter examples (which is false positive from the viewpoint of assertion checking); (3) The abstract state variables in the Extended Finite State Machine (EFSM) model [101] serve as good candidates of decision points in the branch-and-bound process of ATPG. In addition, whenever the search encounters a conflict in an abstract state transition or learns that a transition can lead to a hard-to-reach state, the transition in the Extended State Transition Graph (ESTG) is recorded. This recorded information is then used in the subsequent ATPG process to speed up the search; (4) Compared to the BDD-based symbolic model checking techniques, the proposed method should be much more memory efficient. Both the ATPG-based solver and the arithmetic solver are much less sensitive to the exponential growth of the state space and thus more scalable to larger designs.

3.5.1.2 Automatic Functional Vector Generation for HDL

Several techniques [102][103] have been proposed to automatically generate test vectors for processor designs, but their usage may be restricted on specific architectures. A technique proposed in [104] can automatically generate functional test vectors for HDL designs using the extended finite state machine model. However, it can handle only the simplest statement coverage. A more general solution is proposed in [105] by using a hybrid satisfiability (HSAT) solver. It has good results on the combinational part of HDL designs but may become too computationally expensive for deep sequential designs because it uses the time-frame expansion to handle the sequential part.

In formal techniques, there are many efficient methods to solve the deep sequential problem. Once the binary decision diagrams (BDDs) of a finite state machine (FSM) are built, one can perform a reachability analysis by the BDD operations. Such analysis, which is the kernel of the symbolic model checking [106][107], is still not practical for large designs because of the memory explosion problem of the BDDs. Therefore, suitable partitions to alleviate the peak memory sizes are necessary to handle large designs. Some techniques [108][109] have been proposed to automatically
extract FSMs from the HDL designs. With those techniques, one can represent the HDL designs by the interacting FSM (IFSM) model [110]. The desired state transitions in the monolithic FSM are also partitioned into some concurrent transitions of each small FSM in the IFSM model.

In this research, we shall study an integrated approach which combines the above FSM extraction and symbolic techniques. Because BDD-based techniques are used, it can include all possible patterns in a single BDD instead of only one solution generated in the SAT-based approaches. Most importantly, because the peak memory requirement can be reduced by using the IFSM model and the “divide and conquer” strategy, it can be a practical solution for large designs.

3.5.1.3 State Enumeration Techniques Based On Extended Finite State Machines

Most existing formal verification algorithms [112][113][114][115][116][117][118] suffer from the state explosion problem that is due to the modeling of the entire design using finite state machine models. In this project, we propose to enhance the capability of property checking from two angles: (1) We model the design as a set of interacting Extended Finite State Machines (EFSMs) [111][101]. The EFSM is a more powerful model than the conventional finite state machine and is thus capable of describing complex designs with not only control but also data path components; (2) We shall develop new state space exploration techniques performed on the EFSM models. The state exploration techniques can be often classified into two types – explicit state enumeration [116], and implicit state enumeration [113][118]. We shall investigate the extensions of both of these two state enumeration techniques for the EFSM model. The techniques should be developed should be much less prone to the state space explosion problem than other formal verifiers, and thus should be more scalable for larger designs, thereby making formal verification applicable to practical design blocks. The reasons are two-fold. First, the design intentions are nicely captured in the EFSM model, so that the data which registers irrelevant to the property to be checked are automatically abstracted away. Secondly, highly sequential components such as counters are handled differently from the ones for real state register, and thus do not directly contribute to the state space either. A prototype tool will be developed to demonstrate the effectiveness of the new idea.

3.5.2 Testing (UCSB, Tim Cheng; NTHU, Cheng-Wen Wu)

System-on-chip (SOC) devices usually contain one or more programmable components such as processor cores, DSP cores or FPGA cores. Such programmable resources might be reused for the test purpose. One possible test strategy for a SOC is to utilize these on-chip programmable resources to self-test themselves first. The tested programmable cores can then be used as pattern generators and response analyzers to test on-chip buses, interfaces between cores or even other cores including digital, memory, mixed-signal and analog components.

For faster and deeper submicron technology, self-testing has clear advantages over testing relying on external testers. On-chip clock speed increases dramatically while the tester’s Overall Timing Accuracy does not. This trend implies an increasing yield loss due to external testing since guardbanding to cover tester errors results in loss of more and more good chips [119][120]. Self-testing offers the ability to apply and analyze at-speed test signals on chip with greater accuracy than that available on the tester. In our research, we propose to explore self-test techniques using on-chip resources to target deep submicron defects, especially timing-related defects. We also propose to investigate new test and diagnosis techniques for deep submicron embedded memories.

3.5.2.1 Self-Test and Self-Diagnosis Using On-Chip Programmable Resources

The strategy of using on-chip programmable cores for self-testing actually views testing as an application of the programmable components in the SOC and thus, minimizes the addition of dedicated test circuitry for DFT or self-test. Our research goal is to provide an automated test program synthesis methodology for these applications as well as to understand the capability, capacity and limitations of these test applications.

Existing logic BIST techniques belong to the class of structural BIST. Structural BIST such as the scan-based BIST technique [121][122][123], offers good test quality, but requires addition of dedicated test circuitry (such as full-scan, LFSRs for pattern generation, MISRs for data analysis and test controllers). Therefore, it incurs non-trivial area, performance and design time overhead. Moreover, structural BIST applies non-functional, high-switching random patterns and thus, causes much higher power consumption than normal system operations. Self-testing the devices using an instruction set of on-chip processors has the potential to alleviate these problems. We refer this self-test strategy as a functional self-test or embedded software tester solution.
To apply at-speed tests to detect timing-related faults, existing structural BIST needs to resolve various complex timing issues related to multiple clock domains, multiple frequencies and test clock skews which are unique in the test mode. In contrast, self-testing the devices using instruction sequences allows more natural application of at-speed tests. Delay tests are applied by executing instruction sequences in a similar fashion as normal system operations. Our research thrust is to develop methods for automatic synthesis of test programs which, when executed, result in high delay fault coverage for target delay defects.

Pure functional self-test may or may not give a desired level of test quality. We propose to conduct research to characterize the capability and limitations of functional self-test and gain more insights into how functional self-test can complement structural BIST. We then further conduct new research to study hybrid solutions that combine the strengths of functional and structural self-test.

We shall further extend these functional self-test techniques to self-diagnosis of processor components, as well as systems comprised of programmable components. Self-diagnosis programs using the embedded processor’s instruction set will be generated on-chip to identify the location of an error in the embedded processor, and programmable delivery mechanisms will be developed to apply the diagnosis tests at the operational speed of the embedded processor. We shall further develop on-chip diagnosis techniques for other components in SOC by utilizing the self-diagnosis capabilities of the embedded processor.

3.5.2.2 Analog and Mixed-Signal Self-Test

We further propose to develop efficient self-test techniques that target the analog/mixed-signal components in mixed-signal system-on-chip (SOC) designs. Since digital programmable resources such as DSP or processor cores are commonly available in modern mixed-signal SOC designs, our strategy of mixed-signal self-testing is to utilize such on-chip programmable resources while limiting the use of analog/mixed-signal self-test circuitry. This approach not only enhances the flexibility (as various tests can be applied by using different software DSP routines), but also reduces the amount of dedicated test circuitry for self-testing.

Among the various analog/mixed-signal Built-In Self-Test (BIST) schemes proposed recently, we are particularly interested in the DSP-based BIST approach. In the DSP-based BIST approach, on-chip analog-to-digital (AD) and digital-to-analog (DA) converters are used for analog stimulus generation and response digitization, and DSP processors are used for DSP operations needed to prepare the digitized test stimulus and perform response analysis. This approach is attractive because: (1) the needed DSP resources can usually be found in modern mixed-signal SOC design; and (2) the setup is flexible in that different tests (DC, AC, and dynamic tests) can be applied to the circuit under test (CUT) by modifying the software routines without hardware alternation.

However, it is not uncommon that a mixed-signal SOC has only an on-chip AD or DA converter, but not both, which limits its application. We propose to develop efficient BIST techniques for SOC devices that have on-chip DSP resources but lack an on-chip AD or DA converter. To fully utilize the digital resources, the devised techniques should have the following features:

?? Signal processing for the test execution should be performed by the on-chip DSP resources whenever possible.

?? The use of analog/mixed-signal BIST circuitry should be minimized.

?? The analog BIST circuitry must have robust performance against process variations, i.e., the analog/mixed-signal BIST circuitry won’t fail at the presence of process variations within a reasonable range.

?? One must be able to characterize and test the analog/mixed-signal BIST circuitry relatively easily with on-chip resources and minimum aid from external ATE.

3.5.2.3 Testing of Embedded Memories in SOC

We propose to investigate test and diagnosis techniques for deep submicron, embedded memories. The topics to be explored include fault modeling for new failure modes, vector generation, built-in self-test and built-in self-diagnosis.

New Fault Models for Memories. In DSM memory cores, we need to consider delay faults and interconnect coupling and noise issues as in logic cores. In addition, reliability failures will be harder to deal with, especially for on-chip DRAM, flash-EPROM, and flash-EEPROM. New fault models such as word-line (gate) disturbance faults, bit-line (drain/source) disturbance faults, read disturbance faults, cell endurance faults, and data retention faults need to be addressed.

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Vector Generation for Memories. The March-based test algorithms are considered the most cost-effective for RAM stuck-at, transition, coupling, stuck-open, and address-decoder faults. Traditionally, the development of test algorithms aims at covering as many fault models as possible [119][124][125]. However, with the growing complexity of memory chips, test time reduction is more and more a concern, even for linear-time algorithms. Efficient test algorithms for the ever-innovating memory chips will need to be discovered in a much shorter time than before. Test algorithm generation and verification for RAM is conventionally done using mathematical approaches [126][127][128]. Though elegant, these mathematical approaches do not provide fault coverage figures during the generation and verification process as well as in the background selection steps.

We shall investigate a different approach: testing algorithm generation by simulation (TAGS) [129], which is based on fast memory fault simulation [130]. Given a set of faults, TAGS can generate a series of March tests with different March elements and lengths. It can be used to optimize the test algorithms with respect to test time or fault coverage. We shall also investigate the possibility of using TAGS to generate test algorithms for disturbance, endurance, and retention faults.

Memory BIST and Diagnosis. For memory cores, built-in self-test (BIST) is a relatively mature approach to attacking their test issues [131][132]. In addition to testing the embedded memories using March-based algorithms, diagnosis of the fault sites and subsequent repair by redundant word-and/or bit-lines to increase the yield is necessary for large cores [133][134][135][136][137]. Therefore, built-in self-diagnosis (BISD), built-in redundancy analysis (BIRA), and even build-in self-repair (BISR) methodologies are becoming inevitable, so far as overall test cost is concerned. Diagnosis may also be done for failure/fault analysis. In this case, however, in addition to error location by BIST, fault types should also be identified and classified, followed by required analysis to come up with fault locations.

We shall develop BISD (including BIST) methodology and design technology for embedded RAM (SRAM and DRAM). In association with the BISD design, we also will develop a diagnosis system for off-line failure/fault analysis. The proposed BISD core has a fault-location mode that supports laser repair, and an on-line programming mode for custom test commands. Upon receiving the error location and error signature, the diagnosis system will determine the fault type of every error cell, and provide graphical summaries for the user.

3.6 Collaboration Within the Center

The success of the proposed International Research Center depends heavily on how well various teams across the Pacific Ocean will collaborate. The Center will set up a web-based infrastructure to support collaborative system design and software development. All documentations, current project status, partial results, design driver and design tools under development, etc., will be available to the researchers in the Center via a password-controlled website. Once a certain milestone is achieved, the research results will be made available to the public in a timely fashion through publications and postings on the Center’s public website.

The Center will have three workshops, each of 1 to 2 days, for researchers to have face-to-face meetings to exchange research ideas and results and coordinate various research and development activities. The locations of these workshops will rotate between US, Taiwan, and China (we have included a request to the NSF International Program in the budget to support PIs attending and hosting such workshops). Two workshops have already been held in the course of preparing this proposal (January 27, 2000 in Yokohama, Japan during the ASPDAC’2000, and April 1 to 2, 2000 in Hawaii). Another workshop is scheduled for August 26 to 27 in Chengde, China after ICDA’2000. We also plan to have short-term or mid-term faculty and student visits/exchanges to facilitate further development of the research project.

The researchers involved in the Center have a long history of collaboration. For example, Professors Jason Cong, Youn-Long Lin, and C. L. Liu co-organized an international workshop on “Challenges and Opportunities In Giga-scale Integration for System-on-a-Chip” in August 1999 in Hsin-Chu, Taiwan under the joint support of NSF and NSC. Prof. Xianlong Hong spent the summer of 1995 at UCLA as a visiting researcher and worked closely with Prof. Cong’s group. Prof. Tim Cheng visited NTHU from April 1999 to July 1999, followed by the visit of Prof. Cheng-Wen Wu to UCSB from August 1999 to February 2000. Prof. Wu has collaborated with Prof. Tim Cheng on a low-cost reconfigurable memory tester, test chip design for analog built-in self-test, and processor-based built-in self-test. Prof. ShiYu Huang is currently visiting UCSB and working closely with Prof. Cheng’s group in the areas of functional verification and design error diagnosis. Also, one PhD student from NTHU is visiting UCSB for a period of one year. We expect such close working relationships will continue and further develop through shared vision, common research interests and goals, and frequent interactions in performing proposed research.
3.7 **Educational Impact**

This project will bring the participating graduate students to the research frontiers of IC design and automation. It provides an excellent opportunity to train them as young scientists in the research community and leaders/innovators in the semiconductor and information technology related industries. They will be working on a wide range of leading-edge research problems, from high-performance circuit designs, to giga-scale system integration, to development of novel synthesis and testing algorithms and software tools. This kind of broad research experience will not be easily gained from any classroom setting or regular-size NSF project.

The experience that the students gain from this international collaborative effort will also be very valuable to them and will provide a better understanding of many aspects of the global economy and technology development. The U.S. students will have opportunities to visit the participating institutes in Taiwan and China, and/or work there for a period of time if required by the project. They will have access to some of the best technologies, scientists, and young talents in Taiwan and China. There is a clear trend for globalization, from marketing, to product development, and to advanced research, as evident from the globalization efforts by all major U.S. hi-tech companies. It is very important to train our future scientists and engineers to be well prepared for this new global economy.

3.8 **Results from Prior NSF Supports**

3.8.1 **Research Results from Prior NSF Supports of Prof. Jason Cong**

In the past five years, Prof. Cong has completed one NSF-funded project and has three on-going projects, as listed below:

- "Performance Optimization in Layout and Logic Synthesis of VLSI Systems," NYI Award, $312,5000, 07/93-06/98. (Extended to 08/01)
- "Nonlinear-Programming Based Algorithms for Constrained Circuit Placement" (PI), $85,000, 2/1999 - 1/2001

We shall briefly summarize the research results from these projects in the following subsections.

**Results from “NSF Workshop on Challenges and Opportunities in Giga-Scale Integration for System-On-A-Chip”**

Under joint sponsorship of the U.S. National Science Foundation (NSF) and Taiwan National Science Council (NSC), Prof. Cong organized the International Workshop on Challenges and Opportunities in Giga-Scale Integration for System-On-A-Chip together with Professors Youn-Long Lin and C. L. Liu from the National Tsinghua University, Taiwan. The workshop was held in Hsin-Chu, Taiwan, August 24 to 26, 1999. It was attended by thirteen researchers from U.S., ten researchers from Taiwan, and two observers from NSF. The two-day workshop included a keynote speech by Dr. Chi-Foon Chan, President of Synopsys, presentations by a number of workshop attendees, a field trip to TSMC, the largest IC foundry worldwide, and a number of discussions and brainstorming sessions. This international workshop was held in Taiwan with the active participation of researchers and engineers of Taiwan, because the dominant portion of the world's largest and most advanced integrated circuit fabrication foundries are now located in Taiwan. In the SOC design era, system integration happens at fabrication foundries during IC manufacturing, as opposed to in system houses as in the past. This workshop identified a set of key challenges and opportunities for giga-scale system-on-a-chip integration and divided them into areas of physical design, synthesis, system-level design, programmable components and systems, verification and test. The final workshop report has been submitted to NSF for general distribution and is also available from [http://cadlab.cs.ucla.edu/~cong/nsf_workshop99/](http://cadlab.cs.ucla.edu/~cong/nsf_workshop99/)

**Results from "Performance Optimization in Layout and Logic Synthesis of VLSI Systems"**

This is the NSF Young Investigator Award awarded to Prof. Cong in 1993. Originally, the project focused on “Synthesis and Mapping on Look-up Table Based FPGA Design.” Later, the research scope was expanded to include
various performance optimization issues for general VLSI circuits and systems, and the project was extended to 2001. Many important research results were obtained in this project, and they were presented in over 60 publications, many in the most prominent VLSI CAD journals and conferences, such as IEEE Trans. on CAD, DAC, and ICCAD. We briefly summarize the results into the following areas:

FPGA synthesis; Prof. Cong’s group developed the first polynomial time depth-optimal mapping algorithm for lookup-table based FPGA designs, which received the 1995 IEEE Trans. on CAD Best Paper Award. Continuing the excellence in this area, his group has made signification progress on FPGA synthesis under the support of this project. Recent results include highly efficient algorithms for simultaneous mapping, retiming, and pipelining in FPGA designs [1,7], the first in-depth study of synthesis and architecture evaluation of FPGAs with heterogeneous lookup-tables [4,5], embedded memory blocks [2], and complex programmable logic blocks [3,6].


Interconnect design and optimization: Under the support of this project, Prof. Cong’s group has done extensive and in-depth study on design and optimization of high-speed VLSI interconnects in deep submicron designs, and achieved many interesting and original results, including interconnect topology optimization with buffer insertion [9, 10, 13], optimal wiresizing and spacing [12], high-speed clock net routing [14], novel approaches to interconnect performance estimation and design planning [15], interconnect-centric design flow [16], and so on. For most of these topics, Dr. Cong's group was the first in formulating the problem and providing efficient optimal or near-optimal solutions. Some sample publications include:


Novel approaches to large-scale circuit partitioning: Viewing partitioning as the first step that defines interconnects, which have significant impact on circuit performance in deep-submicron design, Prof. Cong's group has performed extensive studies on new and efficient techniques for circuit partitioning, including use of dual netlist representation [17], use of signal flow based clustering techniques [18], and combination with retiming to hide global interconnect latency [19]. Some sample publications include:


Results from "Nonlinear-Programming Based Algorithms for Constrained Circuit Placement"

This is a joint project with Professors Tony Chan and Joe Shinnerl from the UCLA Mathematics Department aimed at developing novel techniques to handle large-scale circuit placement with complex design constraints in deep submicron designs. Since the project started in late 1998, much effort was spent on developing a multi-level placement engine that uses a hierarchical model of the problem allowing smooth approximations to non-smooth and discrete constraints, uses fast multipole expansions to accelerate evaluation of the constraints and their derivatives, and uses fast numerical solutions to KKT-based systems. The first prototype was completed early this year and encouraging results were obtained. It achieved over 10X speedup with comparable placement results compared to the well-known GordianL package. The result will be reported in:


3.8.2 Research Results from Prior NSF Supports of Prof. Tim Cheng

Three awards were received by Prof. Cheng during the past five years:


The project sponsored by the first award is still in progress and just entering the second year. A brief summary of the results and a selected set of publications resulting from the second and third awards are given below. Under NSF support, we have also written two new books [3][12] which cover recent research as well as a survey of results from other researchers in delay testing [1] and in design debugging and equivalence checking [10].

NSF Workshop on Future Directions in Testing of Electronic Circuits and Systems

The goals of the workshop were: (1) to identify emerging and mature research areas within the VLSI testing field in order to help focus the field on research necessary to develop algorithms and techniques for testing VLSI circuits and systems designed using future technologies, (2) to address issues related to increasing the impact of the VLSI test field on education in electrical and computer engineering, and (3) to identify models and mechanisms for enhancing the interaction, collaboration and data-sharing between industry and academia.
We have formulated the process as a sequence of partial corrections. Each partial correction reduces the size of the input vector to narrow down the possible locations of the errors. For error correction, we use the symbolic BDD techniques to develop a method and a prototype tool for rectifying a combinational circuit that is different from a given specification [9][10]. The logic rectification process consists of two stages: (1) error diagnosis, and (2) error correction.

AQUILA has been developed, which further incorporates local BDD techniques [6]. Fully optimized circuits with several thousands of flip-flops have been verified using our tool. We further address the problem of locating design errors in an erroneous combinational circuit. We developed a fault-simulation-based technique to approximate each signal’s probability of being an error source [7][8]. The new technique offers three major advantages over existing methods. First, unlike symbolic approaches, it is applicable for large circuits. Second, it delivers more accurate results than other simulation-based approaches because it is based on a more stringent condition for identifying potential error sources. Third, it can be easily generalized to identify multiple errors and sequential circuits. Furthermore, we have also developed a method and a prototype tool for rectifying a combinational circuit that is different from a given specification [9][10]. The logic rectification process consists of two stages: (1) error diagnosis, and (2) error correction. For error diagnosis, we identify equivalent internal signals between the specification and the incorrect implementation to narrow down the possible locations of the errors. For error correction, we use the symbolic BDD techniques to formulate the process as a sequence of partial corrections. Each partial correction reduces the size of the input vector.

Reachability Computation Using the Extended Finite State Machine Model and Its Applications

Extended Finite State Machine Model - Analysis and Application [3][13]. We developed an Extended Finite State Machine (EFSM) Model to model high-level designs with both data and control for efficient synthesis and verification. The EFSM model retains many advantages of the finite state machine model while overcoming some major limitations of the traditional FSM model (e.g. state explosion). In this model, the processing of the arithmetic and Boolean parts can be made independent. This allows us to apply techniques such as Ordered Binary Decision Digrams (OBDDs) for Boolean variables while using powerful algebraic techniques for arithmetic variables. This hybrid model has the advantage that it can handle both Boolean and arithmetic variables in the same framework. This eliminates the inefficiency and word-size dependency caused by representing arithmetic variables using a Boolean representation such as OBDDs that are used by most existing verification systems. We have developed theory and algorithms as well as a prototype system for fundamental operations on this hybrid model. We further propose an enhanced EFSM model for representing RTL designs which can be automatically extracted from the HDL codes and formally analyzed for the functional vector generation [13]. It is more general than the EFSM model in [3] so that it can handle designs with mixed data and control more efficiently. We also illustrated how to use this model and combine it with a constraint solver for the RTL design verification [13].

Static Property Checking Using ATPG and BDD Techniques [14]. Static property checking verifies some pre-defined functional design rules such as “bus contention,” “racing condition,” and “don’t-care case.” A static property checker typically uses formal verification techniques to prove that the property is under verification. If the property is proven false, a counter-example is generated for debugging the design. Among the different static property checking approaches, ATPG-based and BDD-based are the most powerful and successful ones. We implement both approaches with several optimization techniques on the same framework such that their performance can be compared. The experimental results show that these two approaches have different strengths and weaknesses in proving the static properties. Furthermore, the results indicate that they often complement each other and therefore a hybrid approach results in better performance. We therefore further propose a static property checker based on combined ATPG and BDD techniques. The experimental results demonstrate that the combined approach produces better results.

Sequential Equivalence Checking [4][5][6], Design Error Diagnosis [7][8] and Logic Rectification [9][10]. We have developed techniques and software tools to address the problem of verifying the equivalence of two sequential circuits. With an attempt to handle larger designs, we modified the ATPG technique for verification and developed an effective algorithm to identify equivalent flip-flops between the two circuits under verification [4][5]. A prototype tool called AQUILA has been developed, which further incorporates local BDD techniques [6]. Fully optimized circuits with several thousands of flip-flops have been verified using our tool. We further address the problem of locating design errors in an erroneous combinational circuit. We developed a fault-simulation-based technique to approximate each signal’s probability of being an error source [7][8]. The new technique offers three major advantages over existing methods. First, unlike symbolic approaches, it is applicable for large circuits. Second, it delivers more accurate results than other simulation-based approaches because it is based on a more stringent condition for identifying potential error sources. Third, it can be easily generalized to identify multiple errors and sequential circuits. Furthermore, we have also developed a method and a prototype tool for rectifying a combinational circuit that is different from a given specification [9][10]. The logic rectification process consists of two stages: (1) error diagnosis, and (2) error correction. For error diagnosis, we identify equivalent internal signals between the specification and the incorrect implementation to narrow down the possible locations of the errors. For error correction, we use the symbolic BDD techniques to formulate the process as a sequence of partial corrections. Each partial correction reduces the size of the input vector.
set producing error responses. Compared with existing approaches, this approach is more general, and thus suitable for engineering change problems.


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Introduction


Design driver


Design Specification


High-Level Synthesis


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**Verification and Test**


[122] [ChLi95] K.-T. Cheng and C.-J. Lin. Timing-Driven Test Point Insertion for Full-Scan and Partial-Scan BIST.


5 Biographical Sketches

5.1 Biographical Sketch of Prof. Jason Cong

EDUCATION
?? Ph.D. in Computer Science University of Illinois at Urbana-Champaign, 1990
?? M.S. in Computer Science University of Illinois at Urbana-Champaign, 1987
?? B.S. in Computer Science Peking University, 1985

PROFESSIONAL EXPERIENCE
?? July 1990 - Present Professor (7/98 - present), Associate Professor (7/94 - 6/98), Assistant Professor (7/90 - 6/94) in the Computer Science Department at University of California, Los Angeles, and Co-Director of the VLSI CAD Laboratory
?? June 1994 - Sept. 1994: Visiting Faculty at Intel Corporation
?? Jan 1986 - July 1990: Research Assistant in the Computer Science Department at University of Illinois at Urbana-Champaign

HONORS:
?? Guest Professorship, Peking University (2000)
?? ACM SIGDA Meritorious Service Award (1998)
?? ACM Recognition of Service Award (1997)
?? National Science Foundation Young Investigator Award (1993)
?? Northrop Corporation Outstanding Junior Faculty Research Award from UCLA (1993)
?? National Science Foundation Engineering Research Initiation Award (1991)
?? Ross J. Martin Award for Excellence in Research from University of Illinois (1989)
?? DEC Fellowship in Computer Science (1988)
?? Best Graduate Award from Peking University (1985)

EDITORSHIP & SERVICES TO CONFERENCES AND SYMPOSIUMS (selected)
?? Associate Editor of IEEE Transaction on VLSI Systems (1999-present)
?? Associate Editor of ACM Transaction on Design Automation of Electronic Systems (1995-present)
?? Guest Editor of IEEE Transactions on VLSI Systems, Special Issues on Field-Programmable Gate Arrays (1997-1998)
?? Program Committee Member (1997-2000), Design Automation Conference (DAC)
?? General Chair (1998), Program Chair (1997), Publicity Chair (1996), Program Committee Member (1995-99), ACM International Symposium on Field-Programmable Gate-Arrays
?? Program Committee Area Chair (1996), Program Committee Member & Session Chair (1993-96), IEEE International Conference on Computer-Aided Design (ICCAD)
Program Co-Chair (1999), Publication Chair (1998), Publicity Chair (1996), Program Committee Member (1994-98), IEEE International Symposium on Low Power Electronics and Design
?? Program Committee Member (1998-2000), International Symposium on Physical Design
?? General Chair (1993), Program Committee Member (1993, 1996), ACM/SIGDA Physical Design Workshop

OTHER PROFESSIONAL SERVICES
?? Member of Advisory Board of ACM SIGDA (1993-1999)
?? Consultant to Intel Corporation (1994-present)
?? Member of Technical Advisory Board of Magma Design Automation (1997-present)
?? Member of Technical Advisory Board of DARPA MCM project at Mentor Graphics (1994-1996)
RESEARCH INTEREST AND PUBLICATIONS

Dr. Cong’s research interests include layout synthesis and logic synthesis for high-performance low-power VLSI circuits, design and optimization of high-speed VLSI interconnects, FPGA synthesis, rapid prototyping, and reconfigurable computing. Currently, he is leading a research group of over 10 Ph. D. students together with several research staffs and M.S. students working in these areas. He has published over 120 research papers and led over 20 research projects funded by DARPA, NSF, and various industrial sponsors in these areas. A complete publication list is available from http://cadlab.cs.ucla.edu/~cong

Five Most Relevant Publications

Five Other Significant Publications

STUDENTS GRADUATED

OTHER COLLABORATORS (in past 36 months)
Tony Chan (UCLA), Andrew B. Kahng (UCLA), C. L. Liu (National Tsing Hua Univ.), Miodrag Potkonjak (UCLA), Majid Sarrafzadeh (Northwestern Univ.)
5.2 Biographical Sketch of Prof. Kwang-Ting (Tim) Cheng

Experience
06/99 - Director, Computer Engineering Program, Univ. of California, Santa Barbara
07/97 - Professor, Department of ECE, Univ. of California, Santa Barbara
11/98 - Executive Committee Member/Test Thrust Leader, MARCO/DARPA Design and Test Focus Center
04/99 - 07/99 Visiting Professor, Department of EE, National Tsing-Hua Univ., Taiwan ROC
11/93 - 06/97 Associate Professor, Department of ECE, Univ. of California, Santa Barbara
08/88 - 10/93 Member of Technical Staff, AT&T Bell Labs., Murray Hill, NJ.

Education
Ph.D. EECS, University of California at Berkeley, California, 1988
(Ranked First in Ph. D. Preliminary Exam)
B.S. Electrical Engineering, National Taiwan University, Taiwan, R.O.C., 1983
(Ranked First in a Class of 183)

Awards
Fellow, IEEE, Jan. 2000

?? Best Paper Award in IEEE/ACM Design Automation Conf., 1999
?? Best Paper Award in IEEE/ACM Design Automation Conf., 1994
?? Best Paper Award in AT&T Conference on Electronic Testing, 1987

Professional Activities
?? Associate Editor, IEEE Trans. on Computer-Aided Design, since Aug. 1992
?? Associate Editor-in-Chief, IEEE Design & Test of Computers, since Jan. 1999
?? Co-Guest Editor, Special Issue on MCM, IEEE Design & Test of Computers, Dec. 1993
?? Co-Founder & Steering Committee Member, IEEE Int’n Test Synthesis Workshop, Santa Barbara, CA 1994-2000
?? Keynote speaker, ”Sequential Circuit Testing - Past, Present and Future,” at CAD/VLSI workshop, Taiwan, March 1992
?? Keynote speaker, 8th Conf. on Design of Circuits and Integrated Systems, Madrid, Spain, November 1998

RESEARCH INTEREST AND PUBLICATIONS
Prof. Cheng’s current research interests include VLSI testing, design synthesis, and design verification. He has published over 150 technical papers, co-authored three books and holds nine U.S. Patents in these areas. He has also been working closely with US industry for projects in these areas. He is currently supervising two postdoc researchers, nice Ph.D. students and one master student.

Five Relevant Publications


Five Other Recent Significant Publications


PAST RESEARCH COLLABORATORS (WITHIN 48 MONTHS)

Dr. Deb. Mukherjee
Dr. Sandip Kundu
Dr. Mike C.J Lin
Prof. Maraget Marek-Sadowska
Prof. Sharad Seth
Dr. Sudipta Bhawmik
Dr. Vishwani Agrawal
Dr. K.C. Chen
Prof. Sujit Dey
Prof. Kaushik Roy
Dr. Srimat Chakradhar
Dr. Janusz Rajski
Dr. John McDermid

ADVISOR AND ADVISEES

Prof. Ernest Kuh, Dr. ShiYu Huang (1997), Dr. Chen-Yang Pan (1997), Dr. Angela Krstic (1998), Mr. Yao Yang (1998), Dr. YiMin Jiang (1999), Dr. Huan-Chih Tsai (1999), Mr. Jan Tofte (1999), Dr. Juan-Lang Huang (1999)
5.3 Biographies of Other Senior Scientists in the Proposed International Research Center (not funded by NSF)

In this section, we provide a brief biography for each senior scientist from Taiwan and China who will participate in this Research Center. Although they are not seeking support from NSF, their experience and credential are important to the success of the proposed international collaborative effort.

**Jinian Bian** graduated from Tsinghua University, Beijing, China in 1970. Since 1999, he has been a professor in the Department of Computer Science & Technology, Tsinghua University. He was a visiting scholar in Kyoto University, Japan from 1985 to 1986, and in Kyushu University, Japan in 1999. He has joined several developing VLSI CAD systems including the PANDA VLSI CAD system, which were national projects in China. He has authored and co-authored over 70 papers and 5 books in his research areas. His research interests include logic-level and high-level design specification, simulation and verification, synthesis and DA systems. He is the TPC member of international conferences ASP-DAC'97, '98, '00 (Japan) and CAD/Graphics'99 (China).

**Xu Cheng**, received his Bachelor and MSc and PhD degrees in computer science and engineering from Harbin Institute and Technology (HIT) in 1988, 1991 and 1994, respectively. Currently, he is a professor of computer science and a supervisor of Ph.D. students at Peking University, the associate chair of the Department of Computer Science and Technology and the director of the Computer Architecture Teaching and Research Group. His research interests include: high-performance microprocessor, instruction-level and thread-level parallelism, optimized compiler, embedded system, system-on-a-chip and hardware/software co-design. So far, he has authored and co-authored over 40 papers and three books in his research areas. In addition, he is the member of Computer Architecture Committee of China Compute Federation (CCF) and a member of CCF Young Computer Scientists & Engineers Forum.

**Xianlong Hong** graduated from Tsinghua University, Beijing, China in 1964. Since 1988, he has been a professor in the Department of Computer Science & Technology, Tsinghua University. He was a visiting scholar in UC Berkeley, UCLA and UCSC from 1991 to 1994. He was the chief and vice chief designer to several VLSI CAD systems including the PANDA VLSI CAD system, which were the national projects in China. He has more than 15 achievement awards from the Chinese Science & Technology Committee, The Chinese Education Committee and the Ministry of Electronics Engineering. He has authored and co-authored over 100 papers and five books around his research areas. His research interests include VLSI layout algorithms and DA systems. He is the Senior Member of IEEE, Chinese Electronics Association and the member of steering committee of ASP-DAC.

**Shi-Yu Huang** Shi-Yu Huang received his BS, MS degrees in electrical engineering from National Taiwan University in 1988, 1992 and Ph.D. degree in electrical and computer engineering from the University of California, Santa Barbara in 1997. From 1997 to 1998 he was a software engineer at National Semiconductor Corp., Santa Clara, investigating the system-on-a-chip design methodology. From 1998 to 1999, he was with Worldwide Semiconductor Manufacturing Corp., designing the high-speed built-in self-test circuits for memories. He joined the faculty of National Tsing-Hua University, Taiwan, ROC., in 1999 as an assistant professor. His research interests are in the area of computer-aided design for VLSI, with an emphasis on design verification. He co-authored a book entitled "Formal Equivalence Checking and Design Debugging" published by Kluwer Academic Publishers in 1998.

**Tingting Hwang** received her M.S. and Ph.D. degrees in computer science from Pennsylvania State University in 1986 and 1990, respectively. She is currently a professor of computer science with the National Tsing Hua University, Taiwan. She is an Associate Editor of ACM Transactions on Design Automation of Electronic Systems (TODATES). She received Distinguished Teaching Awards from National Tsing Hua University in 1994 and 2000. Her research interests include synthesis for high-performance and low-power designs and FPGA synthesis.
Jing-Yang Jou received the B.S. degree in electrical engineering from National Taiwan University, and M.S. and Ph.D. degrees in computer science from University of Illinois at Urbana-Champaign, in 1979, 1983, and 1985, respectively. He is professor and chairman of Electronics Engineering Department, National Chiao Tung University, Taiwan. Before joining Chiao Tung University, he was with AT&T Bell Laboratories, Murray Hill, NJ. His research interests include behavioral and logic synthesis, VLSI designs and CAD for low-power, design verification, and hardware/software codesign. He has been elected to Tau Beta Pi. He was the recipient of the distinguished paper award of the IEEE International Conference on Computer-Aided Design, 1990. He served as the technical program chair of The Asia-Pacific Conference on Hardware Description Languages (APCHDL'97) and has published more than 80 journal and conference papers.

Jenq-Kuen Lee received the B.S. degree in computer science from National Taiwan University in 1984. He received a Ph.D. in computer science from Indiana University in 1992, where he also received a M.S. (1991) in computer science. He has been an associate professor in the Department of Computer Science at National Tsing-Hua University, Taiwan, since 1992. He was a key member of the team that developed the first version of the pC++ language and SIGMA system while at Indiana University. He was also a recipient of the most original paper award in ICPP '97 with the paper entitled “Data Distribution Analysis and Optimization for Pointer-Based Distributed Programs.” His current research interests include optimizing compilers, compilers for embedded systems, compiler optimizations for pointer-based programs, compilers for low-power, and parallel problem solving environments. Dr. Lee has published more than 30 journal and conference papers on compiler optimizations.

Youn-Long Lin received his BS degree in electronics engineering from National Taiwan University of Science and Technology, Taipei, Taiwan, in 1982, and his Ph.D. degree in computer science from the University of Illinois, Urbana-Champaign in 1987. Upon his graduation, he joined Tsing Hua University, Hsin-Chu, Taiwan, where he has served as the Director of the University Computer and Communication Center, the Chairman of the Department of Computer Science, the Secretary General of the university, and the Director of the University Library, and is now a professor of computer science. In 1998-1999, on sabbatical leave from Tsing Hua, he was with Global UniChip Corp., an SOC design foundry, as its chief technical advisor. Professor Lin's primary research interest is in computer-aided design (CAD) of VLSI with emphasis on physical design automation and high-level synthesis. He co-authored the book "High Level Synthesis -- Introduction to Chip and System Design." Professor Lin is currently serving on the editorial boards of the ACM Transactions on Design Automation of Electronic Systems (TODAES), Journal of the Chinese Engineering Society, and the Journal of Information Science and Engineering (JISE). He has been a consultant to the Institute for Information Industry (III), the Industrial Technology Research Institute (ITRI), and the Computer and Communication research Laboratory (CCL). He is an advisor of the Science and Technology Advisory Office, Ministry of Education, R.O.C., and a co-PI of the Chip and System Implementation Center (CIC) program of the National Science Council (NSC), R.O.C. He also serves on Intel's Asia-Pacific Advisory Board and advisory boards of several EDA and consumer electronics startups. Professor Lin co-received the Outstanding Young Author Award from the IEEE Circuit and System Society in 1990 and received the Highest-Honored Research Award from the NSC three consecutive times in 1992, 1994, and 1996. He has been an NSC research fellow since 1998. Dr. Lin is a member of the IEEE Computer Society, the IEEE Circuit and System Society, the IEEE Solid State Circuit Society, and the Association for Computing Machinery.

C. L. Liu received his B.Sc. degree (1956) at the National Cheng Kung University in Taiwan, his S.M. and E.E. degrees (1960), and his Sc.D. degree (1962) at the Massachusetts Institute of Technology. He was on the faculty of the Massachusetts Institute of Technology (1962-72) and the University of Illinois at Urbana-Champaign (1972-98), and is currently President and Professor of Computer Science at the National Tsing Hua University in Hsinchu, Taiwan. He is the author and co-author of seven books and monographs, and over 180 technical papers. His research interests include computer-aided design of VLSI circuits, real-time systems, computer-aided instruction, combinatorial optimization, and discrete mathematics.

Dr. Liu received the IEEE Millennium Medal, and the IEEE Circuits and Systems Society Golden Jubilee Medal in 2000. He also received the IEEE Computer Society, Real Time Systems Technical Committee 1999 Technical Achievement Award (inaugural winner) for his contributions in the area of real time scheduling, and the IEEE Circuits and Systems Society 1998 Technical Achievement Award for his contributions in the area of computer aided design of VLSI circuits. He received an Outstanding Talents Foundation Award in 1998. He is the recipient of the 1994 IEEE Education Medal. He also received the Taylor L. Booth Education Award from the IEEE Computer Society in 1992.
Zeyi Wang graduated with a major in computational mathematics from Xian Jiatong University, Xian, China in 1965 and since then he has worked as a teacher in Tsinghua University, Beijing, China. Currently, he is a professor in the Dept. of Computer Science & Technology. From the middle of 1987 to end of 1988, he was a visiting scholar for algorithm studies of the 3-D device simulation on a parallel machine "Hypercube" in the EE Department of Stanford University. Since the beginning of 1990, he has worked on the algorithm design and software development of the 2/3-D parasitic interconnect parameter extraction in VLSI circuits. He has authored and co-authored over 60 papers; about 15 papers of these were indexed by the SCI and EI. As a director, he completed and manages several projects sponsored by the Chinese National Science Foundation and several U.S. companies. In particular, a 3-D parasitic capacitance extraction software named "B3D", jointly developed by Synopsys Inc. and his group, was released to the international market last year.

Cheng-Wen Wu received the BSEE degree in 1981 from National Taiwan University, Taipei, Taiwan, and the MS and PhD degrees, both in electrical and computer engineering, in 1985 and 1987, respectively, from the University of California, Santa Barbara. Since 1988 he has been with the Department of Electrical Engineering, National Tsing Hua University, Hsinchu, Taiwan, where he is currently a professor. He also has served as the director of the university's Computer and Communications Center from 1996 to 1998, and the director of the university's Technology Service Center from 1998 to 1999. He is a Guest Editor of the Journal of Information Science and Engineering, Special Issue on VLSI Testing. Dr. Wu was the Technical Program Chair of the IEEE Fifth Asian Test Symposium (ATS'96), and is the General Chair of the Ninth ATS (ATS'00). He received the Distinguished Teaching Award from NTHU in 1996 and the Outstanding Electrical Engineering Professor Award from the Chinese Institute of Electrical Engineers (CIEE) in 1997. He is interested in design and test of high-performance VLSI circuits and systems. He is a member of CIEE and a senior member of IEEE.

Allen C.-H. Wu received the BSEE degree in 1983 from Taiwan Institute of Technology, Taipei, Taiwan, the MSEE degree in 1985 from University of Arizona, Tucson, Arizona, and the Ph.D. degree in computer science from University of California, Irvine in 1992. He is currently a professor of computer science at Tsing Hua University, Hsinchu, Taiwan. From 1885-1988, he was a research engineer in the Physiology Department at University of Arizona, Tucson. During 1995-1996, he spent his sabbatical leave as a senior staff engineer at Quickturn Design Systems, Inc., San Jose, California. During 1999-2000, he took a one-year leave as a director of technical marketing at Y Explorations, Inc., Lake Forest, California. He co-authored the book "High Level Synthesis -- Introduction to Chip and System Design." He was the program chair and general chair of the International Symposium on System Synthesis (ISSS) in 1988 and 1999, respectively. He is a guest editor of the Special Session on System-Level Synthesis and Design, IEEE Transactions on Very Large Scale Systems (TVLSI) in 2000. He is a member of the IEEE Computer Society, the IEEE Circuit and System Society, the IEEE Solid State Circuit Society, and the Association for Computing Machinery.

Hongxi Xue graduated from Tsinghua University, Beijing, China in 1962. Since 1995, he has been a professor in the Department of Computer Science & Technology, Tsinghua University. He was a visiting scholar at the University of Toronto Canada from 1985 to 1986. He was the chief engineer of North CAD Company, Beijing, China from 1987 to 1988. He received eight honor certificates (1989 to 1996) from Chinese Educational Committee and Chinese Science & Technology Association for International Olympiad in Informatics. Another Honor Certificate was received from Tsinghua University for excellent teaching work (first-class, 1994 ). He was a program committee member of the International Conference on Computer Aided Design and Graphics (CAD/Graphics), 1993, Beijing, China, and a technical committee member of the 4th International Conference on VLSI & CAD,1995, Seoul, Korea. He has authored and co-authored over 30 papers and six books. His research interests include synthesis, simulation, verification and software/hardware co-design.
6 Budget and Budget Justification

For the proposed research, the requested funding from NSF will support two graduate students and one faculty summer month at UCLA and UCSB, respectively. In addition, we request the support of a half-time Center coordinator, whose responsibility is to coordinate and facilitate the research activities between 15 senior scientists and their students in the Center. His or her responsibilities include setting up and maintaining the Center-wide website, all information exchanges, compiling monthly progress reports, organizing three Center-wide workshops each year, arranging student and faculty visits/exchanges among different research groups within the Center, and all other Center-related administrative tasks. We also request that the budget cover the purchase of one workstation each year in the first three years to gradually replace the existing workstations (three to four years old). In this way, researchers in the Center will have access to good computing resources to manage the giga-scale SOC designs.

We also include $30,000 a year for international collaboration in the Center, mainly to support three workshops each year as proposed in Section 3.6, which will be rotating between the U.S., Taiwan, and China. This includes the cost of hosting one 2-day workshop each year in the U.S. for about 30 attendees (assuming each senior researchers brings a research assistant to the meeting), and eight round-trip airfares (at $1,500 each) for the two PIs and their student researchers to attend the other two workshops in Taiwan and China each year. Lodging and other expenses of the U.S. researchers in Taiwan and China will be covered by the local hosting institutions (under the support of their NSC or CNSF).

National Tsing Hua University and National Chiao Tung University will jointly request support from the National Science Council (NSC) in Taiwan for a total of NT$25,000,000 (equivalent to US $800,000) to support researchers in Taiwan who will participate in the proposed International Research Center.

Tsinghua University and Peking University will jointly request support from the Chinese National Science Foundation (CNSF) for a total of 2,000,000 Yuan (equivalent to about US $250,000) to support researchers in China who will also participate in the proposed Center.

Please note that research costs in Taiwan and China are considerably lower due to the cost of living difference, as well as to the fact that graduate student researchers and faculty members are paid directly by their governments without using project funding.

The combined support of NSF in the U.S., NSC in Taiwan, and CNSF in China will provide adequate support for the proposed research activities of the Center.

Supporting letters from the President's Offices at the National Tsing Hua University in Taiwan, Tsinghua University and Peking University in China stating their commitment to the proposed International Research Center on SOC designs are appended in Section 9.
7 Current and Pending Support
8 Facilities, Equipment and Other Resources

The UCLA work will be mainly carried out in the **VLSI CAD Laboratory** in the Computer Science Department. The VLSI CAD laboratory is distributed into two large office spaces, each hosting over 15 graduate student researchers, and a set of regular-size offices for the senior research staff and related visitors. It has space to host two to three visiting students and one to two visiting senior researchers year-round related to this project. The VLSI CAD Laboratory is equipped with over 25 SUN, HP, and NT workstations, plus a newly established workstation room with 16 NT workstations donated by Intel Corporation. The VLSI CAD Lab has much electronic design automation (EDA) software provided by major EDA vendors (such as Cadence and Avant!) and FPGA vendors (such as Xilinx and Altera) under their university program for synthesis, layout, simulation, and FPGA designs. The VLSI CAD Lab has also complete Microsoft software.

All workstations in the VLSI CAD Lab are connected to the Computer Science Department’s local area network (LAN), which in turn connects to UCLA’s main network. The LAN is implemented with a gigabit backbone and 10/100 autosensing switched connections to the desktop. Additionally, the departmental network is connected to the UCLA campus backbone via an ATM connection. The departmental network provides many additional computing facilities, including a large workstation room with 40 machines and a digital design laboratory with 10 workstations available to all graduate student researchers.

The **Testing, Verification and Synthesis Lab at UCSB** contains workstations, equipment and extensive commercial CAD and test software to support research and development on methodologies, algorithms and tool development, as well as to support prototype hardware chips and boards. The CAD systems used in this lab including tools from Cadence, Synopsys, Mentor Graphics, Xilinx and Verplex.
9 Special Information & Supplementary Documentation – Copies of Letter of Intent from Participating Universities in Taiwan and China