

EDA Challenges in Systems Integration

J. A. G. Jess

NSF EDA Workshop

July 8 and 9, 2009

Why should IC-EDA and Electronics Systems Manufacturers move closer?

- With Moore's Law electronic systems move to become IC's – off-chip communication moves on-chip facing IC designers with systems communication legacy
- Electronics Systems market is roughly six times the market of IC's – interesting for EDA to have the ESM's as customers

Two Paradigms: Heterogeneous - Homogeneous

heterogeneous

homogeneous

Many specialized (optimized) compute engine types

Computing

A few (at times frequently replicated) general compute engine types (X86 API,...)

Many specialized “communication fabrics”

Communication

A few universally used standard bus protocols (PCIe, AMBA AXI,...)

Many different memory types, designer in control of memory policy

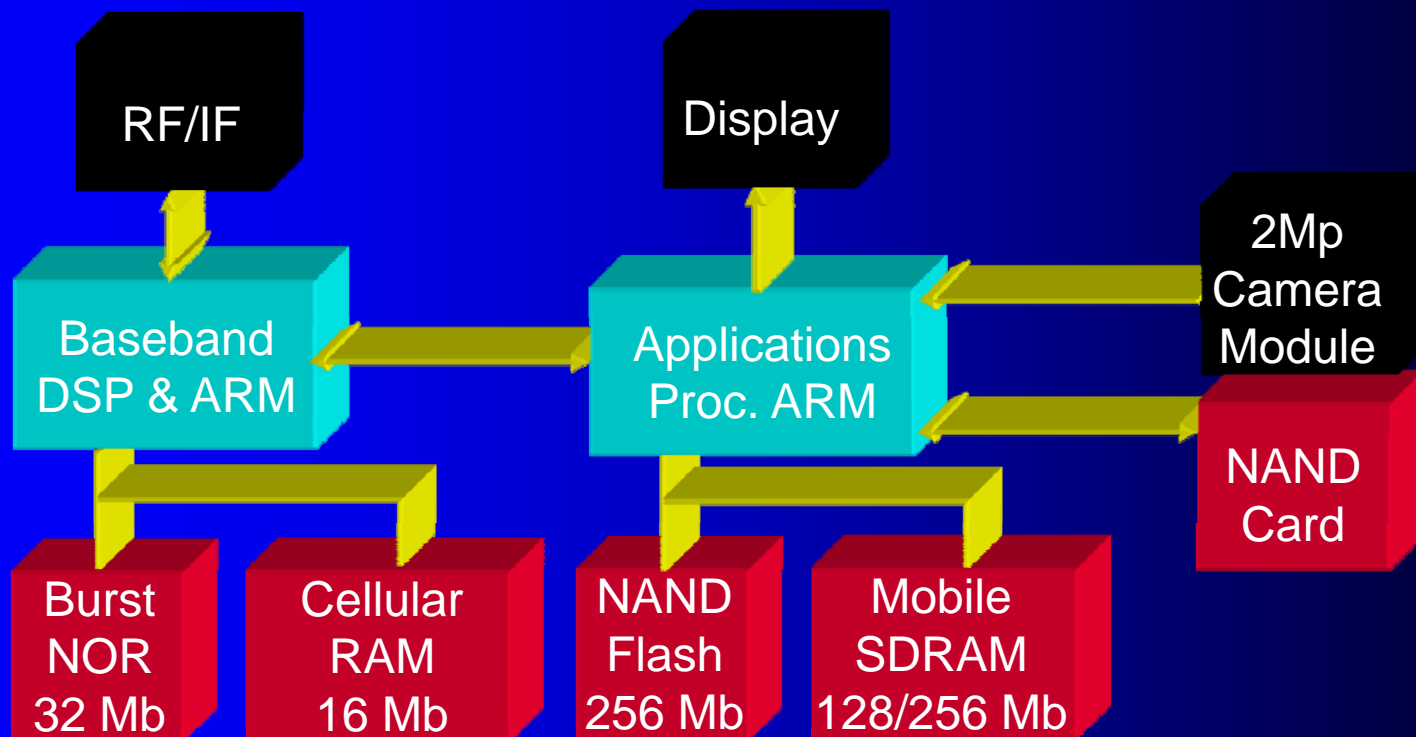
Memory

Standard (virtual) Random Access Memory supported by caches

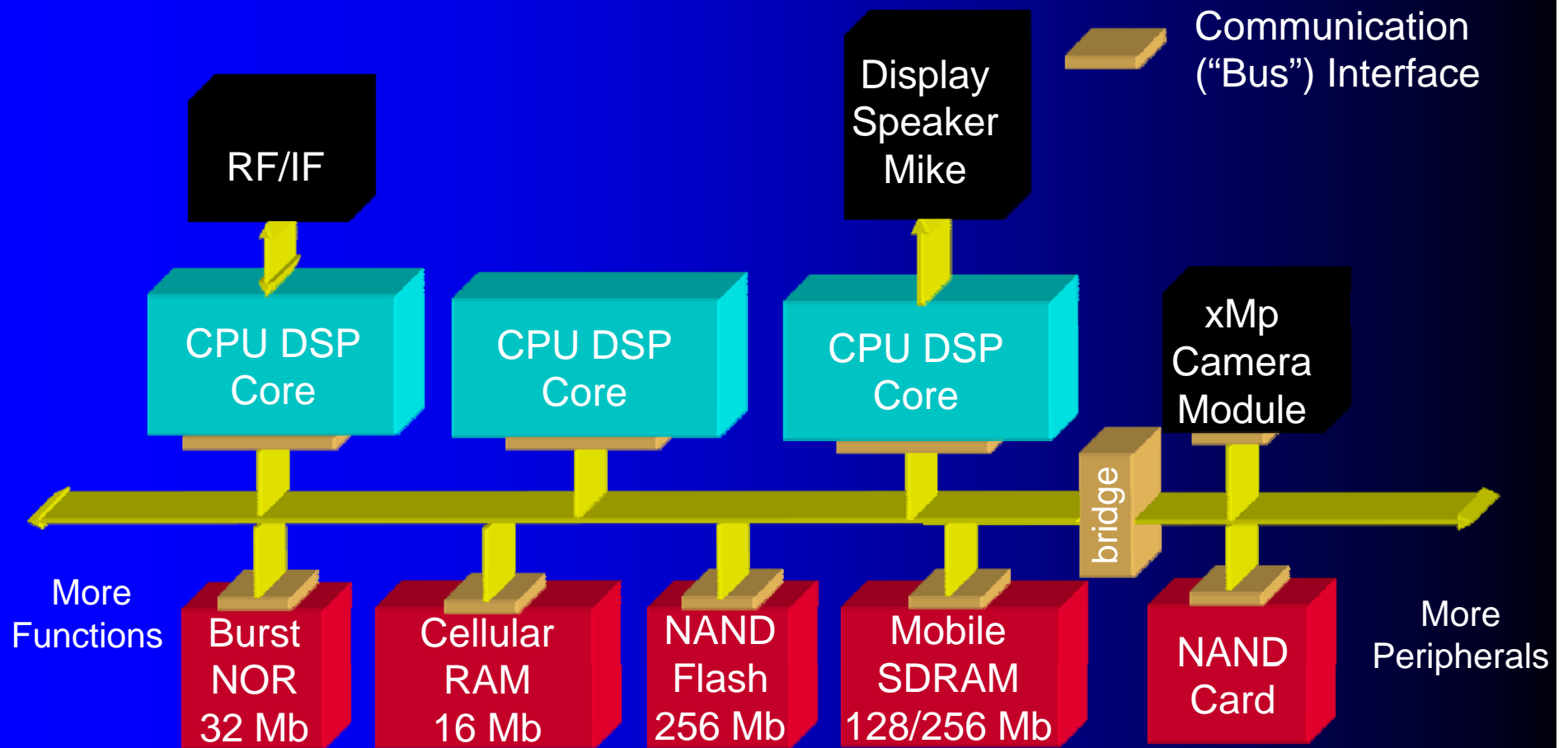
Attempt of a Taxonomy

Heterogeneous	Homogeneous
<ul style="list-style-type: none">● Good Compute Performance to Power Ratio (MOPs/Wsec)● Small “Bill of Material” (BoM, e.g. area)	<ul style="list-style-type: none">● Compute Performance to Power Ratio medium (improving!) but unpredictable● BoM medium to large
<ul style="list-style-type: none">● Lack of Flexibility● Large NRE cost, limited re-use	<ul style="list-style-type: none">● Very flexible through programming on “Virtual Machine”● Extensive re-use of SW and HW

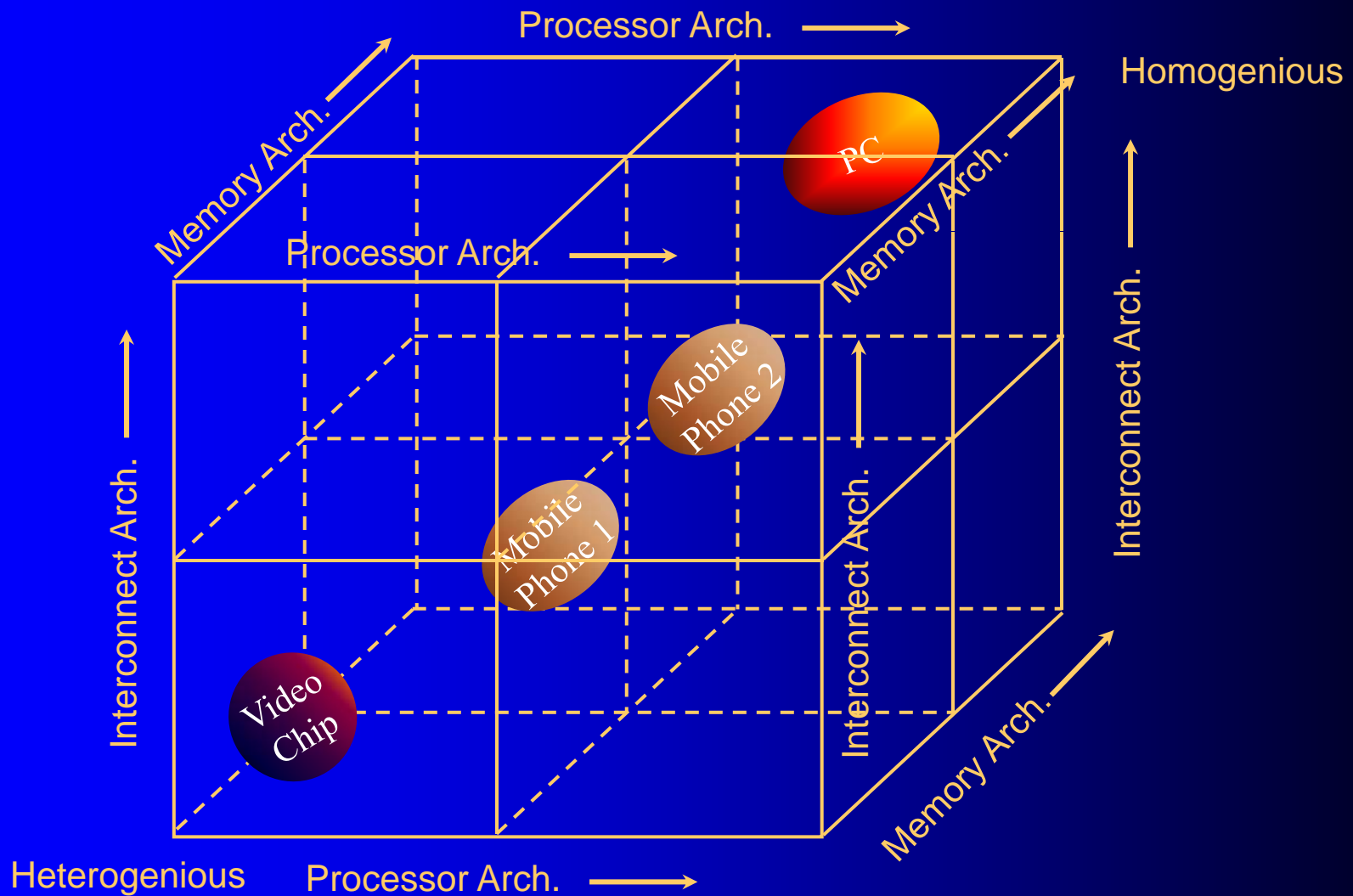
Sample Hardware Architecture Mobile Device (~2005)



Devices sharing Interconnect



Heterogeneity vs. Homogeneity



Basic Challenges

- How to assign performance metrics to the co-ordinates of the cube?
- Given those metrics, how to establish tools providing decision support for designers (and roadmap makers)?

“Systems Integration”

- A large portion of the design effort is concerned with matching the on-chip and inter-chip communication- and memory performance with the specifications
- Communication is critical for Timing and Power
- How deal with contention on shared interconnect?
- Stability of system modes and mode-transitions?
- Verification is hampered by the lack of formal design documentation on system level
- Up to now there seems to be little tooling support – lots of manual code development & guessing

Thank you!