EDA Challenges in Systems Integration

J. A. G. Jess
NSF EDA Workshop
July 8 and 9, 2009
Why should IC-EDA and Electronics Systems Manufacturers move closer?

- With Moore’s Law electronic systems move to become IC’s – off-chip communication moves on-chip facing IC designers with systems communication legacy
- Electronics Systems market is roughly six times the market of IC’s – interesting for EDA to have the ESM’s as customers
Two Paradigms: Heterogeneous - Homogeneous

- **Heterogeneous**
  - Many specialized (optimized) compute engine types
  - Many specialized “communication fabrics”
  - Many different memory types, designer in control of memory policy

- **Homogeneous**
  - A few (at times frequently replicated) general compute engine types (X86 API, …)
  - A few universally used standard bus protocols (PCIe, AMBA AXI, …)
  - Standard (virtual) Random Access Memory supported by caches
Attempt of a Taxonomy

<table>
<thead>
<tr>
<th>Heterogeneous</th>
<th>Homogeneous</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Good Compute Performance to Power Ratio (MOPs/Wsec)</td>
<td></td>
</tr>
<tr>
<td>• Small “Bill of Material” (BoM, e.g. area)</td>
<td>• Compute Performance to Power Ratio medium (improving!) but unpredictable</td>
</tr>
<tr>
<td>• Lack of Flexibility</td>
<td>• Very flexible through programming on “Virtual Machine”</td>
</tr>
<tr>
<td>• Large NRE cost, limited re-use</td>
<td>• Extensive re-use of SW and HW</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Sample Hardware Architecture Mobile Device (~2005)

- RF/IF
- Baseband DSP & ARM
  - Burst NOR 32 Mb
  - Cellular RAM 16 Mb
- Applications Proc. ARM
  - NAND Flash 256 Mb
  - Mobile SDRAM 128/256 Mb
- Display
- 2Mp Camera Module
- NAND Card
Devices sharing Interconnect

RF/IF

CPU DSP Core

Display Speaker Mike

xMp Camera Module

Burst NOR 32 Mb

Cellular RAM 16 Mb

NAND Flash 256 Mb

Mobile SDRAM 128/256 Mb

NAND Card

Communication ("Bus") Interface

More Functions

More Peripherals
Heterogenity vs. Homogenity

Processor Arch.

Memory Arch.

Interconnect Arch.

Heterogenous

Processor Arch.

Memory Arch.

Interconnect Arch.

Homogenous

Processor Arch.

Memory Arch.

Interconnect Arch.

Video Chip

Mobile Phone 1

Mobile Phone 2
Basic Challenges

- How to assign performance metrics to the co-ordinates of the cube?
- Given those metrics, how to establish tools providing decision support for designers (and roadmap makers)?
“Systems Integration”

- A large portion of the design effort is concerned with matching the on-chip and inter-chip communication- and memory performance with the specifications.
- Communication is critical for Timing and Power.
- How deal with contention on shared interconnect?
- Stability of system modes and mode-transitions?
- Verification is hampered by the lack of formal design documentation on system level.
- Up to now there seems to be little tooling support – lots of manual code development & guessing.
Thank you!