Test and Validation in the Late-Silicon Era

Tim Cheng

Electrical and Computer Engineering

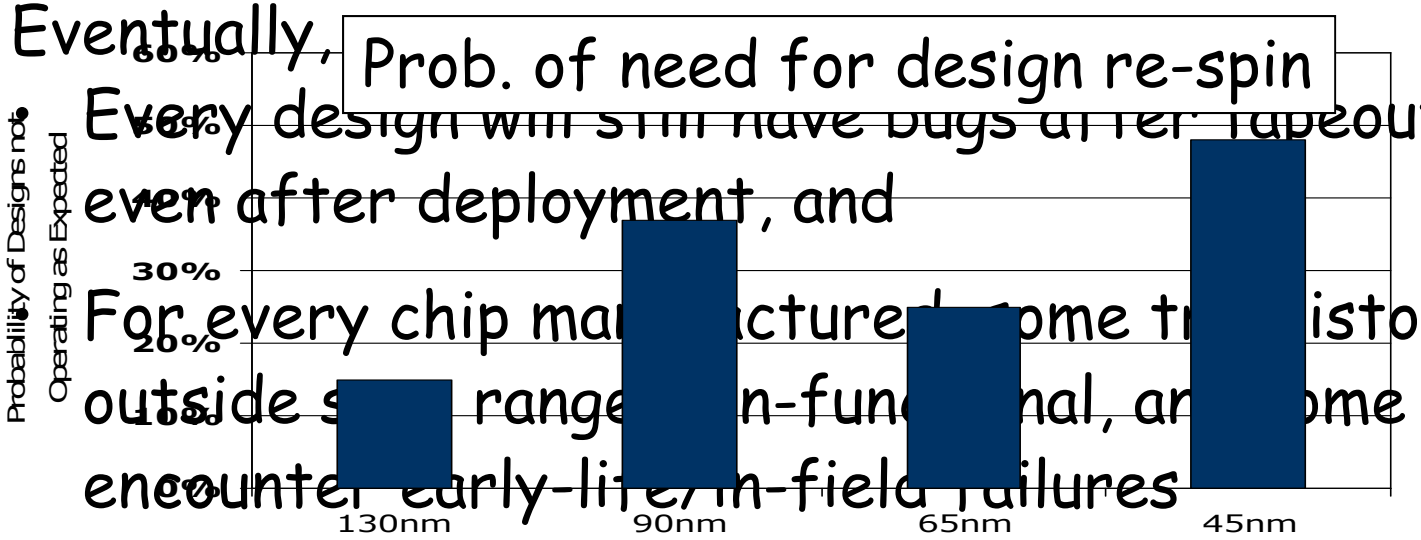
University of California, Santa Barbara

Harder to Produce Working Chips

- First-silicon success rate has been dropping
- Yield has been dropping for volume production and takes longer to ramp up the yield
- "Better than worst-case" design results in failures w/o defects – adding more burden on testing

Eventually,

- Every design will still have bugs after tapeout and even after deployment, and
- For every chip manufactured, some transistors are outside specified range, non-functional, and some encounter early-life/in-field failures



Source: IBS 2007

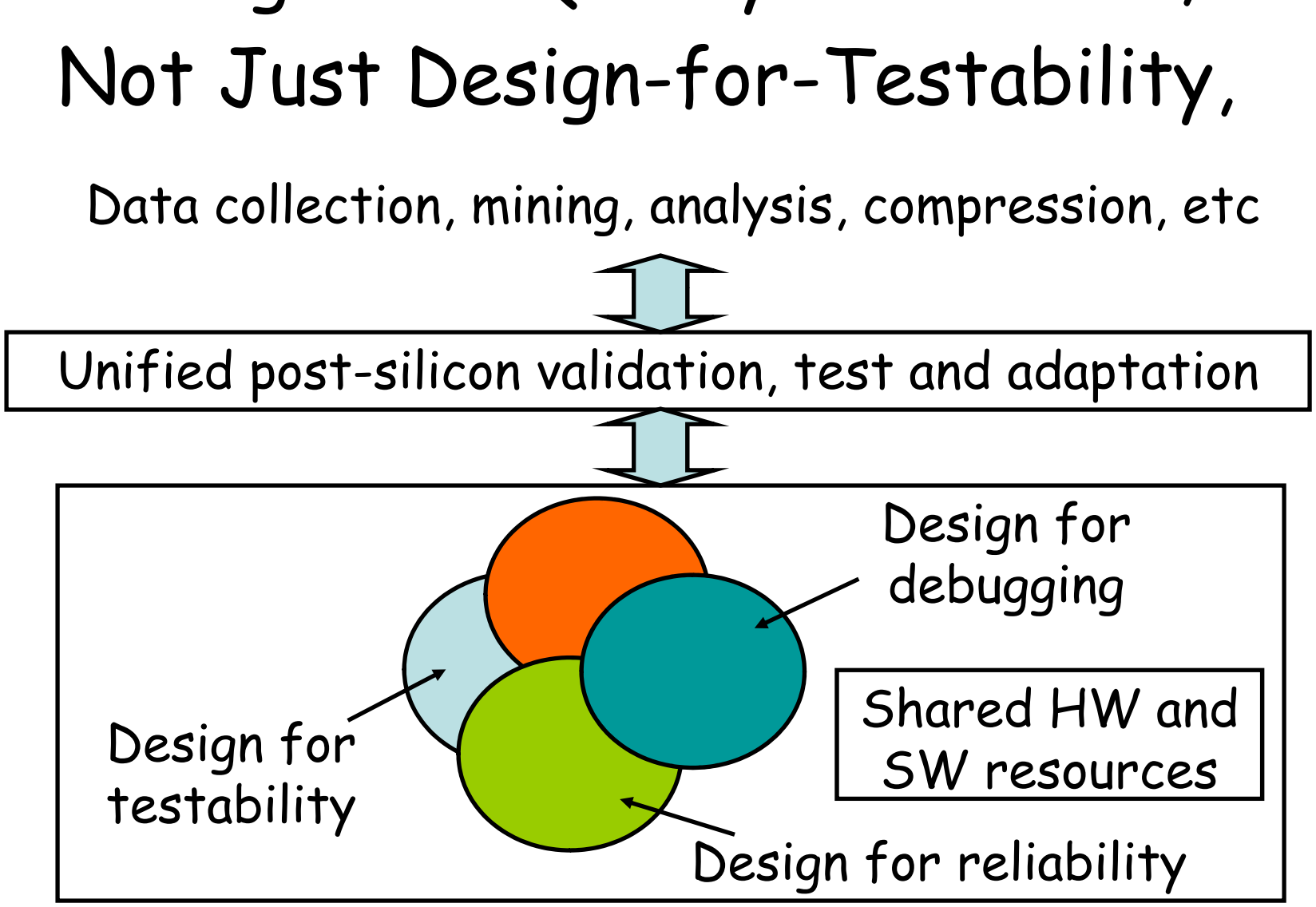
Cost-Effective Production of Working Chips

Chips must be designed to cope with failures:

- Redundancy for error masking
- Spares/Reconfigurability/Adaptability for error recovery
- Embedded self-test for error detection
  - Both on-line and off-line testing
  - For both manufacturing testing and in-field testing
- Supporting heterogeneous, mixed-signals chips (logic, memory, high speed IO, RF, converters, etc.)

Increase reliance on post-silicon validation for bug removal

Design-for-Quality-Assurance, Not Just Design-for-Testability,



Optimization: Sharing HW/SW Resources Among All Post-Si Quality Assurance Functions

- How to generalize design-for-debugging circuitry for runtime validation?
- How to extend embedded validation monitors for on-line testing?
- How to reuse off-line calibration circuitry for in-field on-line calibration?
- How to share off-line BIST and on-line checking circuitry?
- How sensors for detecting early-life failures or wearout can be minimally extended to sense useful silicon data for silicon validation and manufacturing testing?

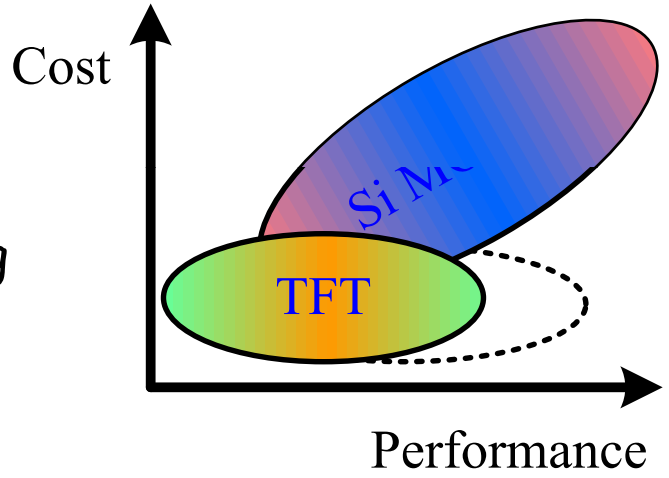
New Problems to Address

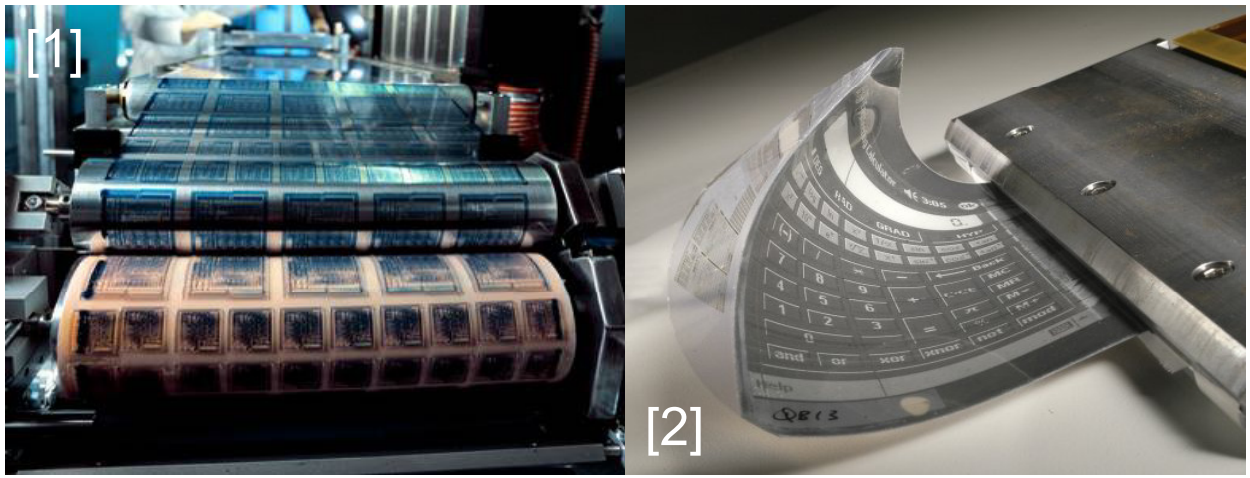
- Validation and testing of error-resilient designs

- Validation and testing for power
  - In contrast to validation/test for functionality, performance, and reliability

What is Flexible Electronics

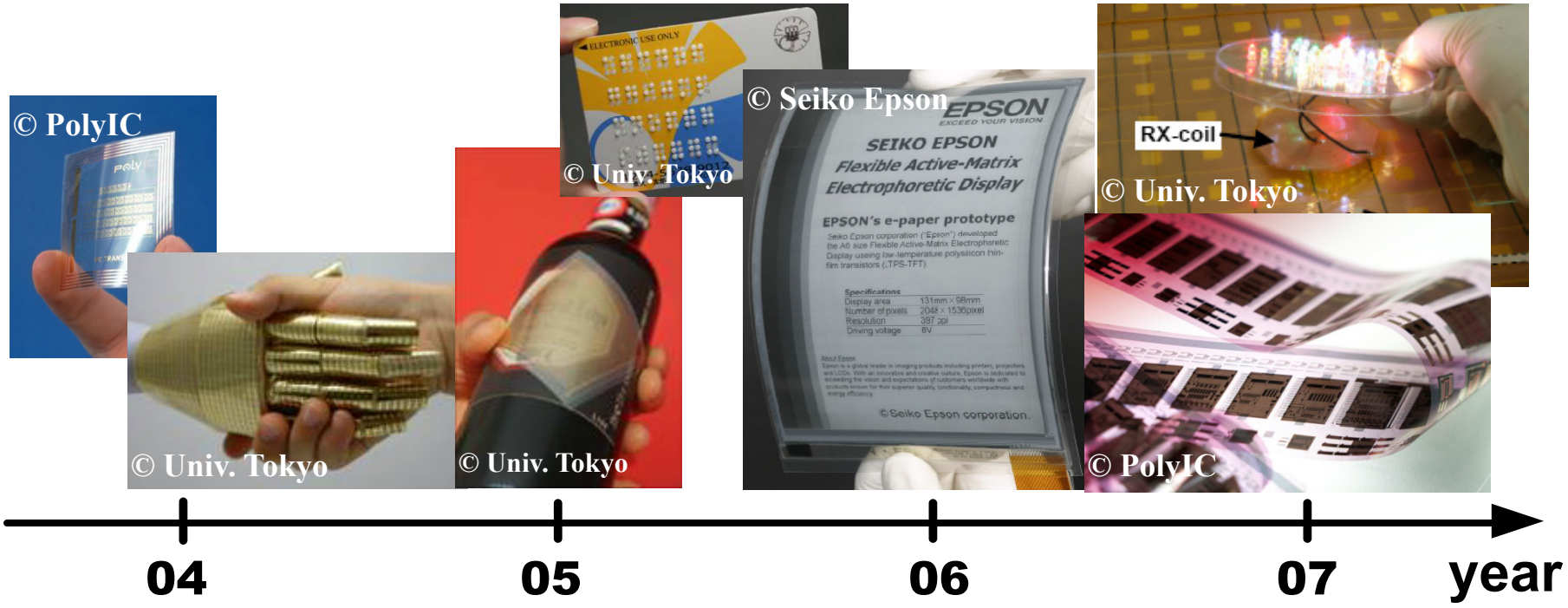
- Thin-film, light-weight, and low-cost
- Bendable, durable, and large-area
- Flexible substrates
  - Plastics and metal foils
  - Non-photolithography manufacturing
    - Ink-jet printing
    - Reel-to-reel imprinting





[1] Roll-to-roll process, PolyIC; [2] Ink-jet printed electronics, Phillips

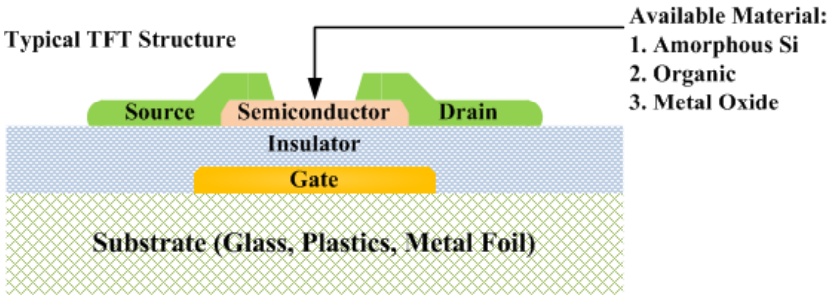
Applications of Flexible Electronics



- Applications
  - Non-destructive structure detectors
  - Flexible solar cells
  - Flexible displays
  - Biometrics — Lab-on-Chip
  - Wearable electronics and displays

Key Difference with CMOS

	Si MOSFET	A-Si:H TFT	Organic TFT	Oxide TFT
Process Temperature	1000 °C	250 °C	Room Temp.	150 °C
Process Technology	Photo-lithography	Photo-lithography	Roll-to-Roll / Ink-Jet	RF Sputtering
Min. Length	<= 65 nm	10 μm	50 μm	10 μm
Substrate	Si Wafer	Glass /Plastic	Plastic/ Metal Foil	Glass /Plastic
Device Type	N- & P-type	N-type	P-type	N-type
Mobility	1500 cm^2/V-s	1 cm^2/V-s	0.5 cm^2/V-s	> 10 cm^2/V-s
Cost/Area	High	Medium	Low	Low
Lifetime	Years	Months	Weeks	Years



Current R&D Efforts for FE

	Device	Circuit	EDA	System
a-Si:H TFT	+++	+	+	-
Metal Oxide TFT	+++	+	-	-
Organic TFT	+++	+	-	-

Technology development mainly focusing on:
1) lower cost, 2) higher yield, 3) faster speed

Still demanding for:
1) Better reliability, 2) lower operation voltage,
3) smaller process variations

EDA Research Opportunities for Reliable Flexible Electronics

- Reliability simulation platform*
  - Reliability analysis, modeling, and simulation
- System solutions for reliability enhancement**
  - Robust design using unreliable devices
  - Post-manufacturing self-test and self-tunable design
- Design-for-printability for roll-to-roll process
  - Substrate-aware physical design methodology
  - Self-aligned layer-to-layer patterning

- Huang et al," Reliability Analysis for Flexible Electronics: Case Study of Integrated a-Si:H TFT Scan Driver," DAC 2007.
- Huang and Cheng, "Design for Low Power and Reliable Flexible Electronics: Self-Tunable Cell-Library Design," Journal of Display Technologies, 2008.