A Flat Earth for Design and Manufacturing

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The Olden Days: Rules-Driven DfM

Design Rule Value (width, space, area, ...)

- Exploit the gap between minimum and recommended rule values
- This has worked well for several generations and will continue for 32nm

Life is Becoming More Difficult: Physical Effects

Lithography

Chemical-Mechanical Polish

Rapid Thermal Anneal
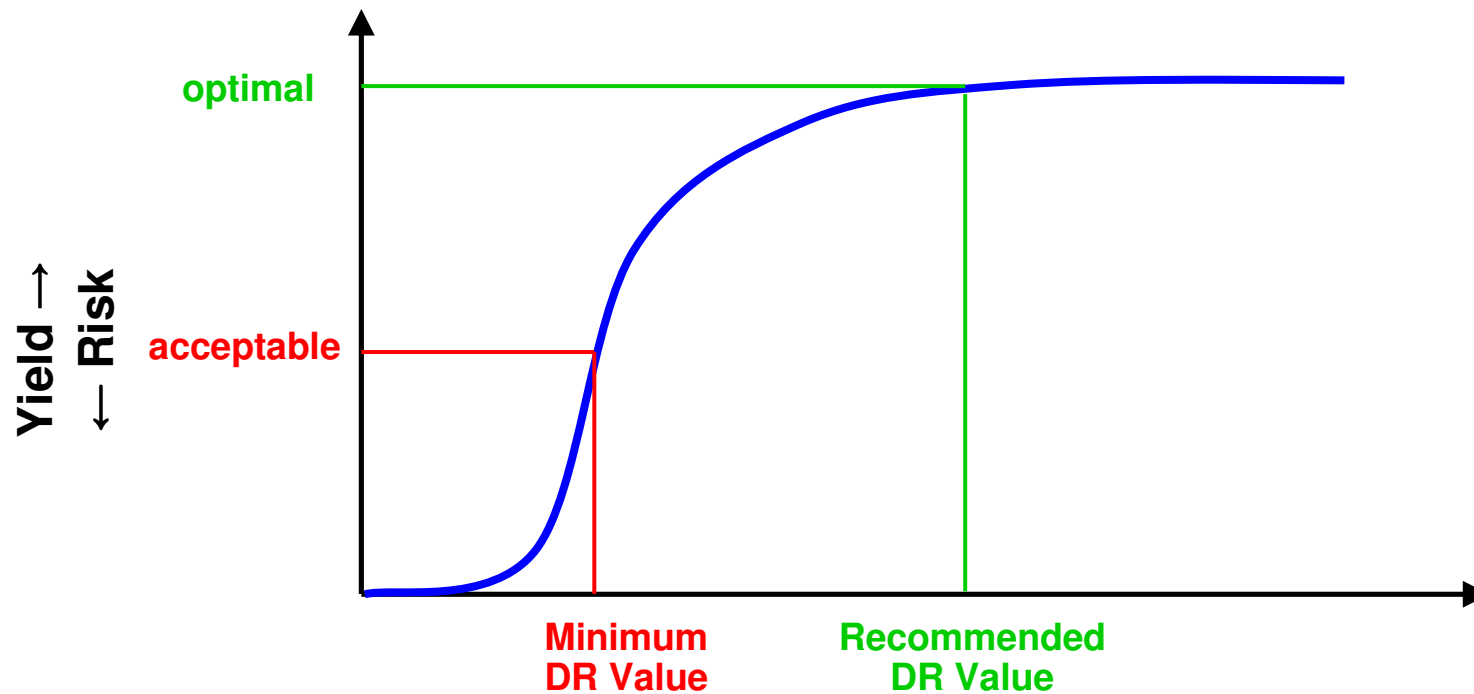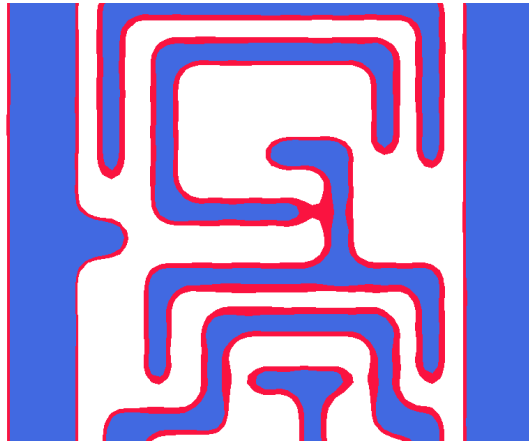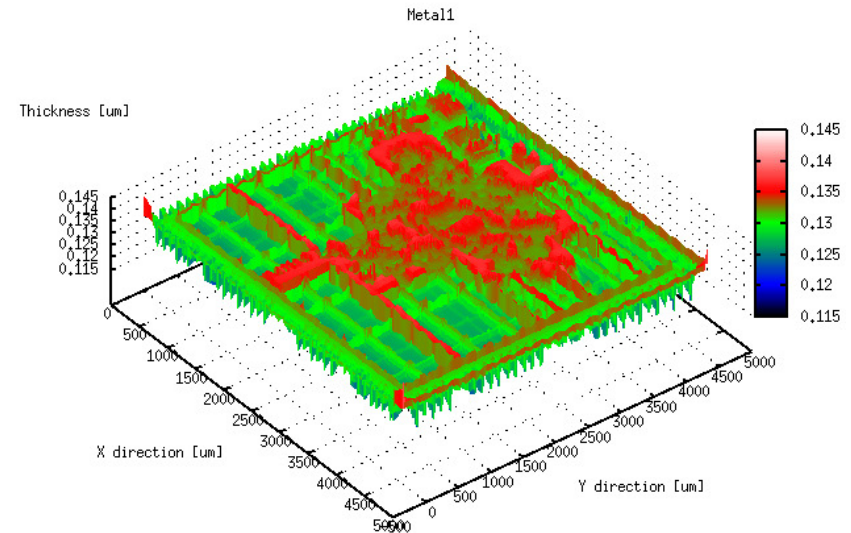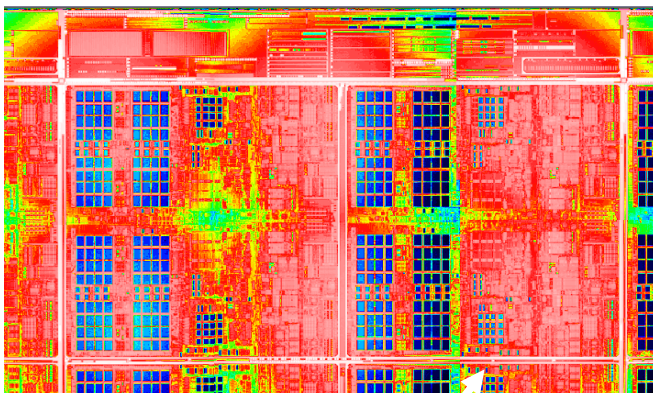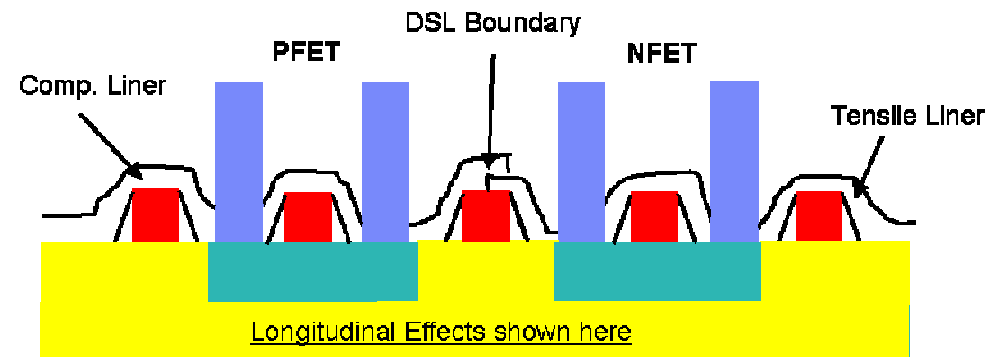
~2% reflectance

Strained Silicon

IBM Systems and Technology Group

Life is Getting Difficult: The Lithographic Picture

Node	90nm	65nm	45nm	32nm	22nm
Year	2003	2005	2007	2009	2011
Pitch	250nm	200nm	140nm	100nm	70nm
λ	193nm				
NA	.75	.85	1.2	1.35	
% of Scaling	74%	39%	97%	26%	0%
Exit Pupil					
k_1	.5	.44	.44	.35	.25
	conventional	annular	annular	quadrupole	dipole
RET	Rigorous Optical Proximity Correction				
	Assist Features				
				Double Patterning & SMO	
Yield vs Pitch	vert. horiz.		$$\text{Resolution} = k_1 \frac{\lambda}{NA}$$		
DfM		Opportunistic DfM		Complex Rules	RDR

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Prescriptive Design

- Rules have become too complicated
  - ➢ and behavior has become non-monotonic

- So instead of *describing* the technology – either through rules or models – let's instead *prescribe* what should be done
  - ➢ through restricted design rules (RDRs)
  - ➢ through pre-qualified patterns

- We will be able to build only a few things well
  - ➢ let's accurately describe the things we can build
  - ➢ so that Design sees accurate models of hardware
  - ➢ and so that Manufacturing sees an accurate representation of desired electrical behavior
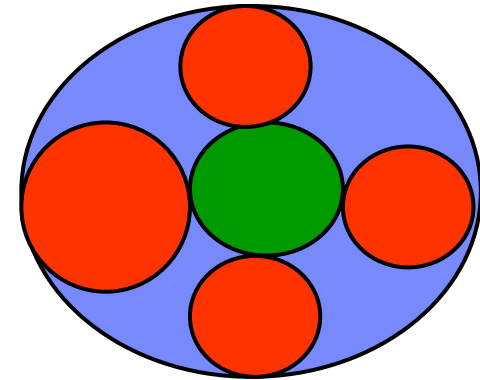
Moving Past DfM: Design-Rule Taxonomy
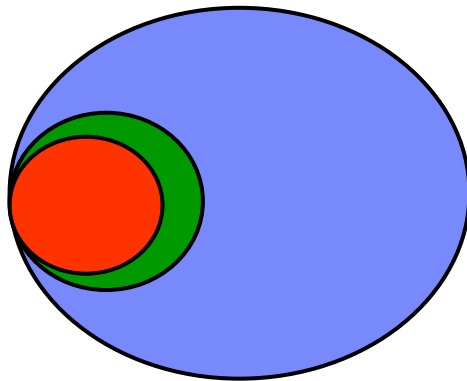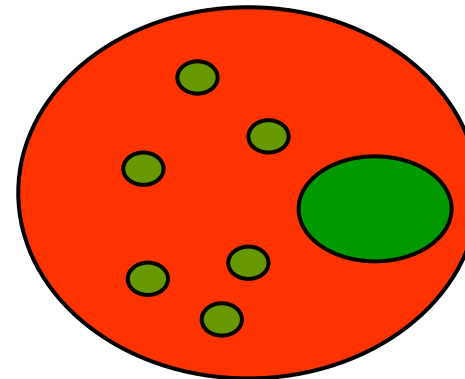
Conventional design rules I
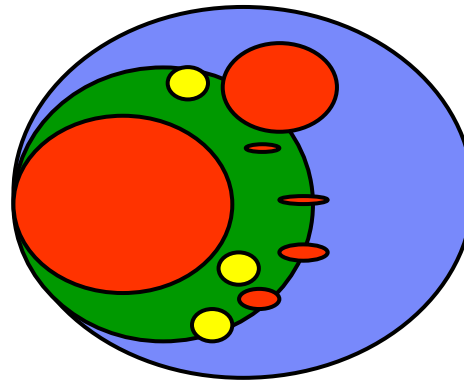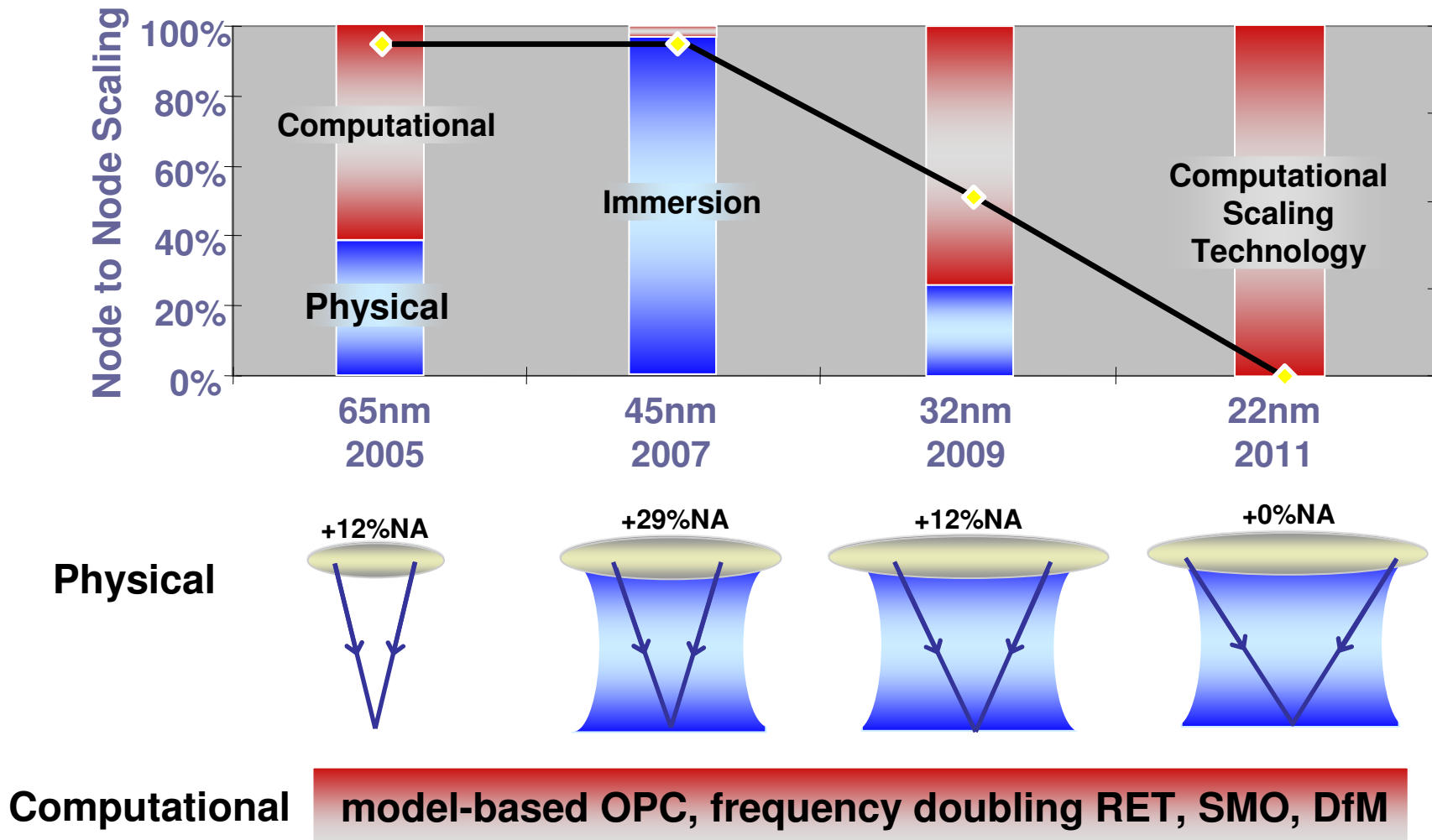
Conventional design rules II

Restricted Design Rules
(prohibitive)

Design Space

Forbidden by rules

Used

Forbidden by models

Restrictive Design Rules
(prescriptive)

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Computational and Physical Efforts Keep Litho Scaling Alive

Node to Node Scaling

100%
80%
60%
40%
20%
0%

Computational

Physical

Immersion

Computational Scaling Technology

65nm 2005
45nm 2007
32nm 2009
22nm 2011

Physical

+12%NA   +29%NA   +12%NA   +0%NA

Computational model-based OPC, frequency doubling RET, SMO, DfM

Math, Science … and Future Challenges

Statistics
- timing
- variability and predicability
- yield estimation

Boolean algebra
- logic synthesis
- formal verification

Mathematical optimization
- yield optimization
- performance tuning
- routing
- double patterning

Physics
- device modeling, lithography, materials

**Our field's tools
of today…**

Template-based design

Double patterning

EUV

**…will have to address
the challenges of tomorrow**