Collaborative Innovation of EDA, Design, and Manufacturing

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2009/7/8
Semiconductor Market Facing Difficult Times

Source: SIA (2009)
But...More Silicon Identified in Future Products!

Source: Gartner, iSuppli, Strategy Analytics (2009)
More than Moore: Diversification

More Moore: Miniaturization

Low Dimensional Materials Channels

Multiple gate MOSFETs

+ III/V High µ Alternative Channel Mat’s

Beyond CMOS

Baseline CMOS: CPU, Memory, Logic

130nm
90nm
65nm
45nm
32nm
22nm

Interacting with people and environment

Non-digital content System-in-package (SiP)

Combining SoC and SiP: Higher Value Systems

Information Processing

Digital content System-on-chip (SoC)

Nanowire Electronics

Ferromagnetic Logic Devices

Spin Logic Devices

Through Silicon Via

Package on Package

Die Stacking

Source: ITRS (2009)
Process Technology R&D

Financial threshold getting higher

Source: tsmc (2009)
System Chip Design

Source: Global Unichip (2009)
Expensive Design Leadership

Source: IBS (2008)
Technology Alliance as One Solution

IMEC

AMD
TOSHIBA
SONY
NXP
ST
INTEL
SAMSUNG
Matsushita
tsmc
Texas Instruments

國立清華大學
National Tsing Hua University
Paradigm Shift for Contract Manufacturing

Sufficient revenue (~ 5B USD) required to support research and manufacturing investments

Source: tsmc (2009)
A Foundry’s Collaboration Model (tsmc)

Open Innovation Platform™

TSMC Innovations
- Process
- Design IP
- Packaging
- Enablement Interface
- Compatibility

EDA tools
- Design IP
- Services

Ecosystem Partner Innovations

TSMC Innovations
- Active Accuracy Assurance
- TSMC Quality Management

Open Innovation Platform
- Solutions Services Flows Tools IP
- Hosted by TSMC

Customer Innovations
- Design Projects
- Design Projects
- Design Projects

Product Tapeout

Source: tsmc (2009)
Growing Concerns

- Technology Leadership
  - Logic: Intel; Memory: Samsung
  - Foundry technology offering behind Moore’s Law
  - High cost for fabless to adopt leading edge technology
- Skyrocketing cost for advanced litho & uncertain roadmap
  - Hardware suppliers hesitate toward 450mm infrastructure
- Market dominated by tool vendors and manufacturing service
- University labs: limited process technology researches
- Constrained university-industry collaboration: IP concerns
- Imbalanced university researches between process/device & design/EDA
Collaboration for Industry’s Total Innovation

• Innovative collaboration models to share R&D cost
• Government plays a crucial role
  – Initiate and support “national R&D programs” to help regional industries
  – Encourage international/industrial collaborations to leverage global research network
• Topics for EDA research (computation intensive)
  – Manufacturing: yield ramp-up
  – 3D-IC: modeling, design, manufacturability
  – Multicore SoC: software quality and design productivity
  – Energy efficiency: generation, distribution, consumption
  – …
Example “National R&D Drives” (Taiwan)

- **Telecom (since 1998):** ~ US$ 70M/yr
  - Wireless, Broadband Internet, Telecom Services, ...
- **SoC (since 2001):** ~ US$ 70M/yr
  - IC (RF, Mixed-Signal, DSP), Embedded S/W, EDA
- **Nanotechnology (since 2003):** ~ US$ 100M/yr
  - Nano-materials and nano-fabrications
  - For applications in semiconductors, optoelectronics, bio-medical, energy, ...

International & industrial collaborations are highly encouraged and supported in university programs!
Conclusion

- Semiconductor industry is facing historical challenges
- Need innovative collaboration model to share R&D cost
- Government role is crucial
  - Initiate and support national R&D drives
  - Encourage and support university programs for international and industrial collaborations