NSF Workshop:
Electronic Design Automation—Past, Present, and Future

Analog CAD: Not Done Yet

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The Mixed-Signal Design Problem

% Design Effort

Digital

Analog

Commercial Mixed Signal ASIC
Total worldwide market for non-memory ICs in 2008: **$167B**

- Mixed-signal portion (has some analog/RF) was **$107B** in 2008 – about **66%**
- Projected to grow to **70+%** in 2012
- Growth rate **higher** than overall non-memory IC marketplace
Context: State of the Art for Synthesis

- Give me a circuit with ~100 devices, we can
  - **Help** quickly size, optimize for perform/yield, layout, compact, migrate ...
  - First-generation, emergent industrial tools, from several sources
  - Tools far from perfect, but workable across range of designs

STMicroelectronics result

[Shah, Dugalleix, Lemery DATE02]

<table>
<thead>
<tr>
<th>Size</th>
<th>Area</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.18um</td>
<td>0.009 mm²</td>
<td>9.15 mW</td>
</tr>
<tr>
<td>0.12um</td>
<td>0.004 mm²</td>
<td>1.1 mW</td>
</tr>
</tbody>
</table>

Both sizing and layout

[Source: Cadence]
Bigger Example: Design Migration

TOSHIBA

Porting an SOC data converter (180nm to 140nm)

~10X less design time

Design Time (Days)

180nm Manual

140nm Auto

[Source: Cadence]
What 1st-Gen Tools Got Right: Optimization-Based

- All successful approaches formulate the solution as some form of “deep” optimization (not a bag of random circuit heuristics)

- Use some clever form of combinational/numerical search
  - Optimization engine: proposes candidate circuit solutions
  - Evaluation engine: evaluates quality of each candidate
  - Cost-based search: cost metric represents “goodness” of design

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What Did We Not Get (Entirely) Right...?

- **Constraint extraction and tradeoff management**
  - Critical stuff in real designs often *never written down*
  - Exists *implicitly* in design group's legacy portfolio and human resources

- **Integration: functional, electrical, geometric, etc**
  - Design steps much less independent than digital
  - Usually optimizing across *N steps simultaneously*
Constraint Extraction/Mgt: Industrial Example

- Proprietary CMOS comparator block
  - Lots of critical electrical / geometric constraints – none of them explicit on schematic, all extracted (arduously) from interaction with designer

- Opportunity: Constraint “harvesting/mining” from good designs
Reducing these “barriers” to use is a huge, very real problem

(Can’t just ask circuits designers to stop complaining – it’s our problem to solve)
Opportunity: Every Step In Every Flow: Fast, Incremental, and Deterministic

- Need very fast “what if…” for all electrical/geometric steps
  - Incremental is not how these “deep optimizer” algorithms are done today
  - Req for fast+deterministic is also a huge challenge (but essential for usability)

Note – these are not std cells. Small Δs here can have big, bad impacts on overall ckt
Design is almost always a high-dimensional set of pareto tradeoffs, and many goals are really soft (or negotiable...)

- Means you can waste vast amounts of time trying to optimize something that is impossible, when you should have been presenting tradeoff info...

Just like that...but better.
Opportunity: Incremental Tools + New Use Models

- Adobe Photoshop offers an interesting vision of this
  - This is "Image variations"
  - A palette of incremental changes to base image

- Can I do this for analog?
  - For critical analog metrics?
Opportunity: Unified Optimization Steps

- Even in digital, it’s not really: RTL $\rightarrow$ Logic $\rightarrow$ Place $\rightarrow$ Route
  - For timing, for power, for yield, many intermediate, adjustment, repair steps

- Same true for analog – but tend to happen more concurrently
  - This is the downside of focusing on designs that all fit on ONE screen

Lots of opportunities to do the same step-spanning optimizations that experts do
Summary

- Lots of progress
  - Real deployment and use
  - Improving usability, integration

- But: Not done yet, not close
- Lots of big, new challenges