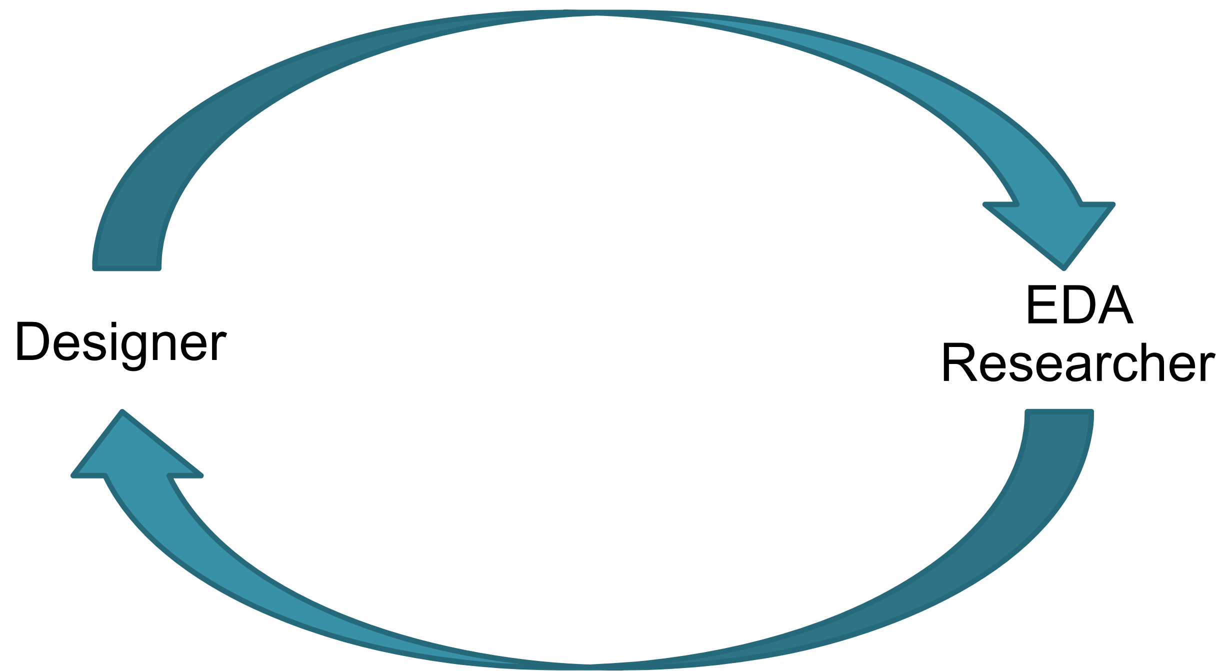
Mary Jane Irwin, Penn State

NSF Workshop: Electronic Design Automation – Past, Present, and Future

July 8 and 9, 2009

Abstract

-
- The design constraints of improved performance, better energy efficiency, increased reliability, and constrained design costs challenge EDA researchers as silicon technology continues to scale according to Moore's Law. However, there are functions that our "standard" silicon technology – CMOS – just doesn't do well. For functions such as global interconnects, on-chip non-volatile memory, and massive (high bandwidth) input/output, technologies other than CMOS combined with 3D integration holds great promise. For example, a network-on-chip in a second layer exploiting optical and/or RF technology can provide high performance, energy efficient, and reliable global interconnects. SRAM/DRAM memory stacking allows massively parallel memory access helping to mitigate the memory wall and dramatically reducing the large off-chip memory energy consumption. Additionally, stacking emerging non-volatile memory which is immune to radiation-induced soft errors can provide on-chip non-volatile storage while consuming zero standby power. Stacked layers of chemoresistive sensors, mass-sensitive nanoresonators, and biologically-selective FETs fabricated via a directed-assembly approach can provide radically new input/output mechanisms.
-
- But to achieve the promise of 3D integration as a way to sustain Moore's law as well as to enable More-than-Moore requires advances by the EDA community working with the design community, as well as interdisciplinary efforts with chemist, biologists, and material scientists. Fundamental research challenges for the designer include determining a functional partitioning that maximizes the benefits of vertical connections while achieving optimal performance and energy efficiency, designing the interface circuitry between the CMOS "brains" and the non-CMOS technologies, and ensuring temperature stability across and between layers. To meet these challenges, design methodologies and design tools necessary to implement and simulate/validate 3D architectures which integrate these new technologies and must be developed.

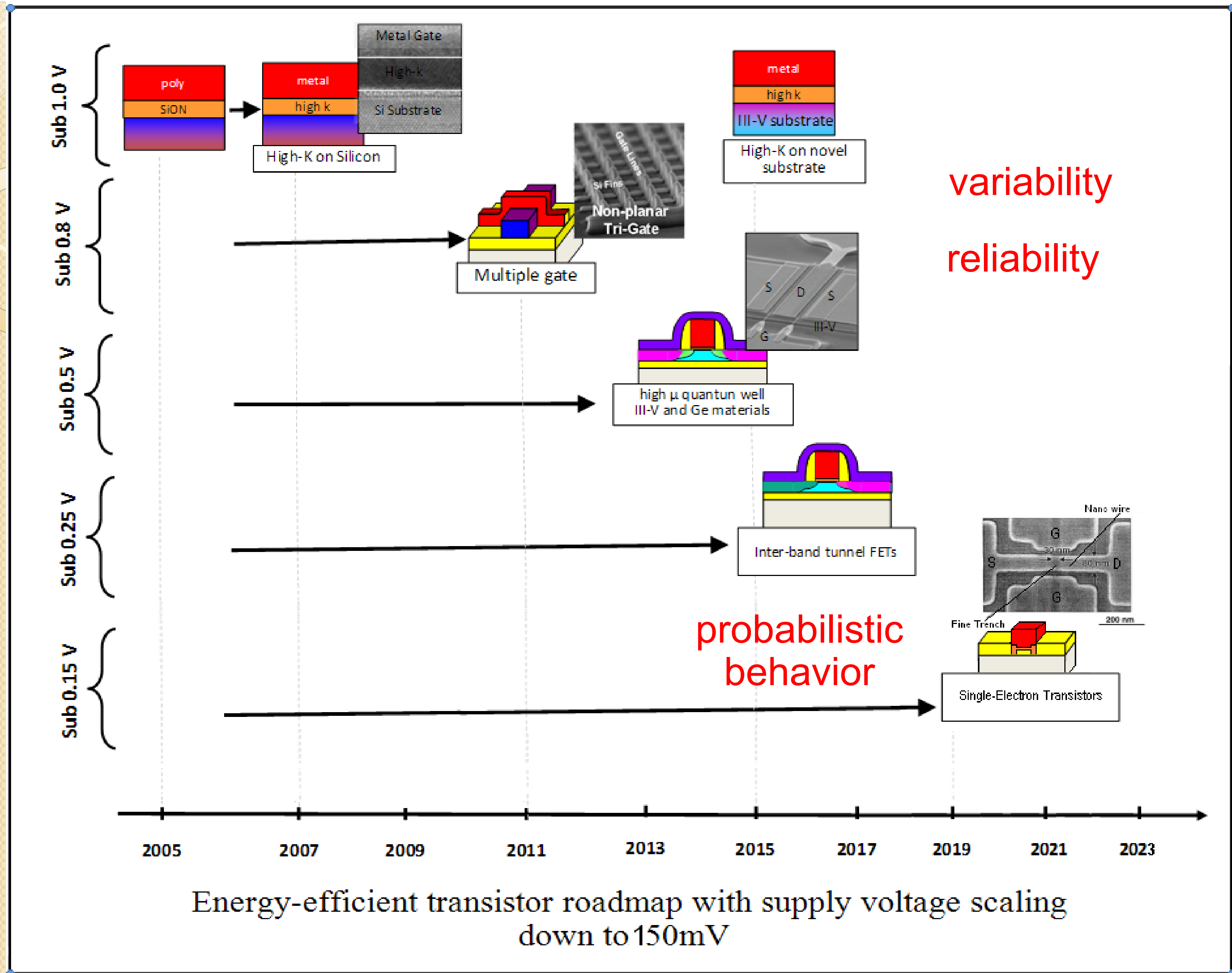

Designer
EDA
Researcher

Bookkeeping fabric

- No need to be blazingly fast
- “Old” CMOS suffices (>250nm)
  - Better reliability
  - Less leakage
  - No or little process variation
  - Existing tools (mostly) work fine

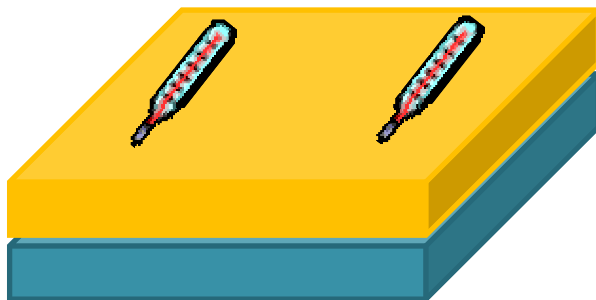
Adding compute power fabric

- Take advantage of scaling for compute power (<90nm)
- Now highly susceptible to faults, variation, leakage, etc.
  - Must be dynamically reconfigurable
  - Must have to have a way to monitor the "health" of the compute elements



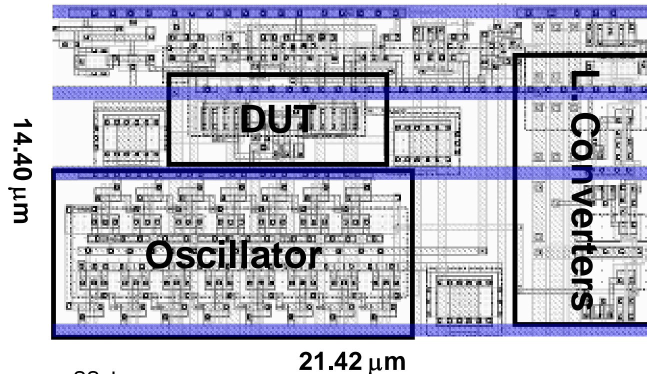
Picture of SET PADOX Structure : Fabrication method for IC-oriented Si single-electron transistors Ono, Y.; Takahashi, Y.; Yamazaki, K.; Nagase, M. Namatsu, H.; Kurihara, K.; Murase, K.

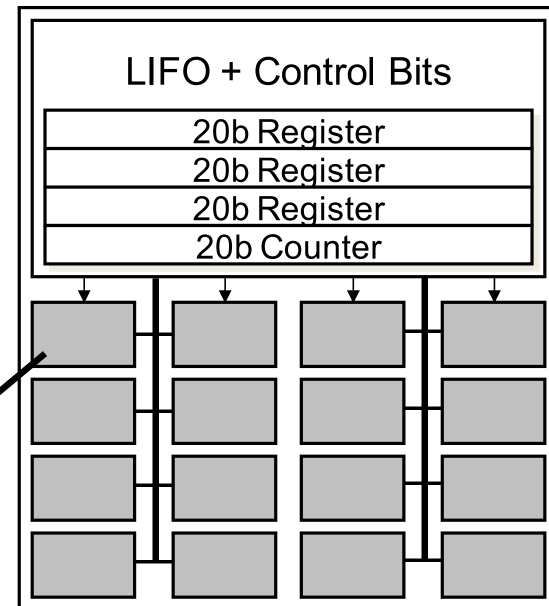
Monitoring the compute fabric

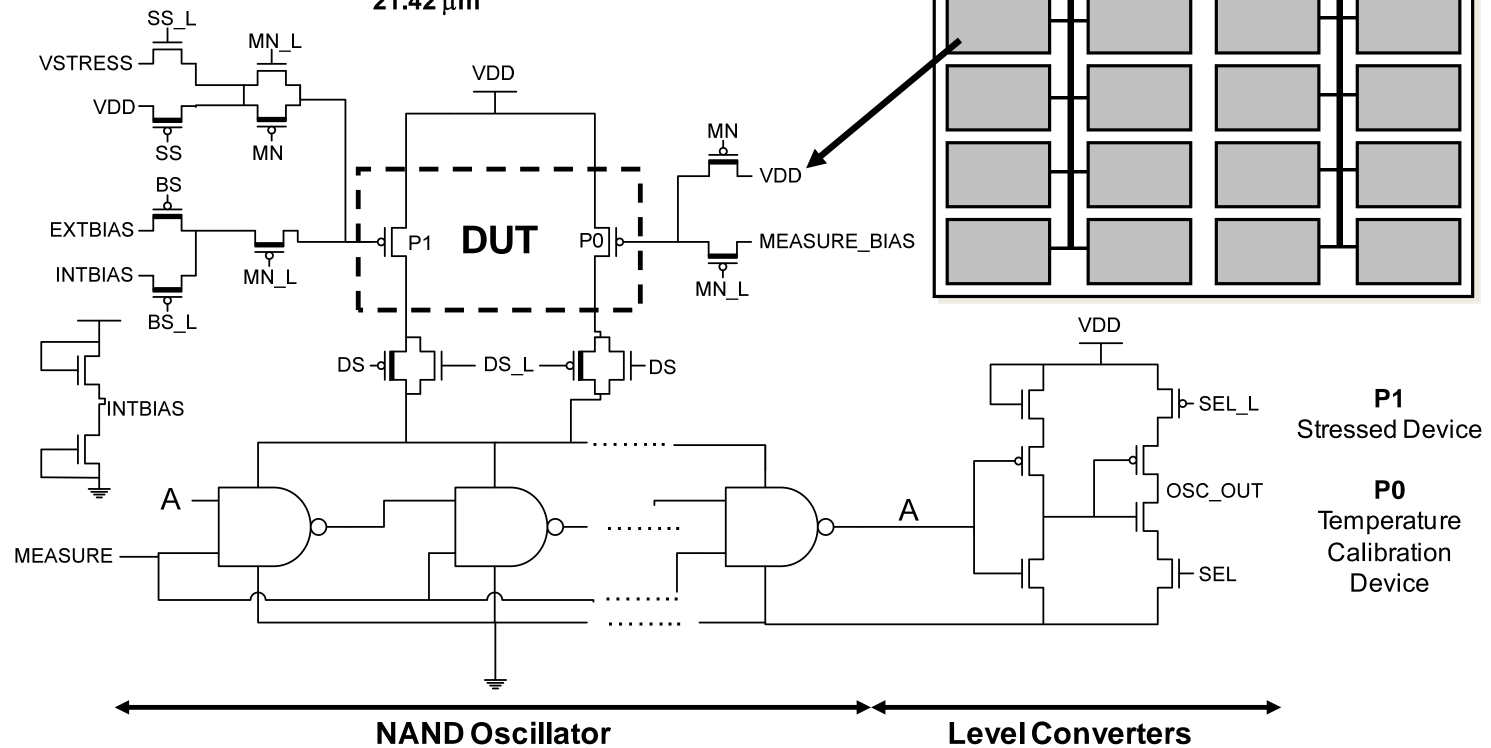


- Performance/power/ fault "sensors"
  - Hardware counters
  - Temperature sensors
  - …
- Control knobs
  - Turn off idle and faulty cores & links
  - Apply DVFS
  - …

NBTI and oxide wearout sensors



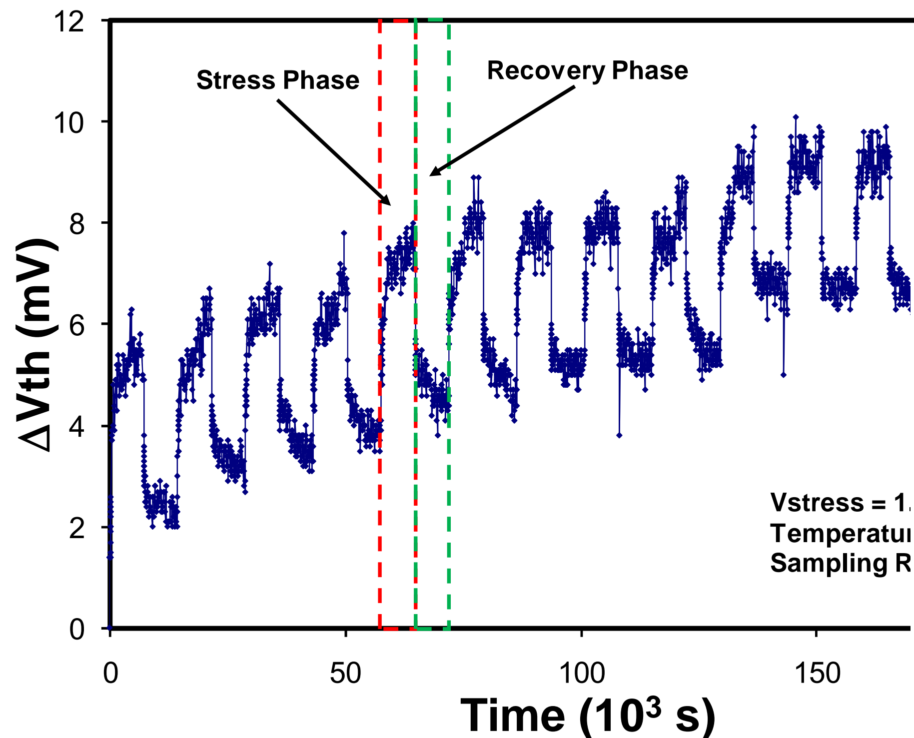




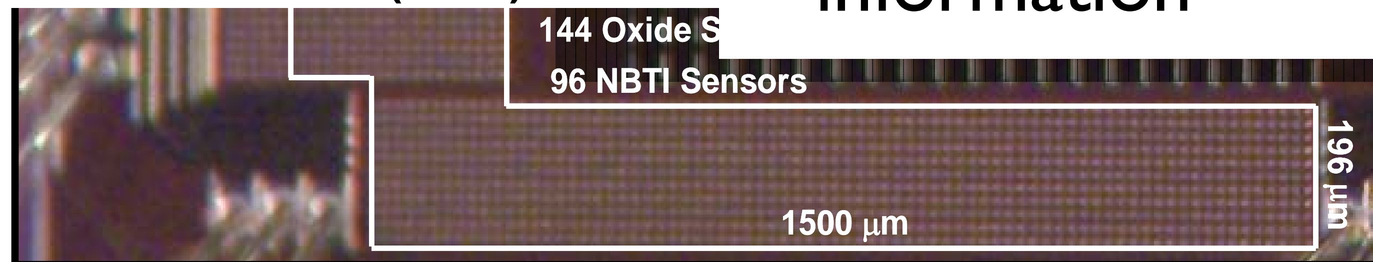
P1
Stressed Device

P0
Temperature Calibration Device

NBTI sensors

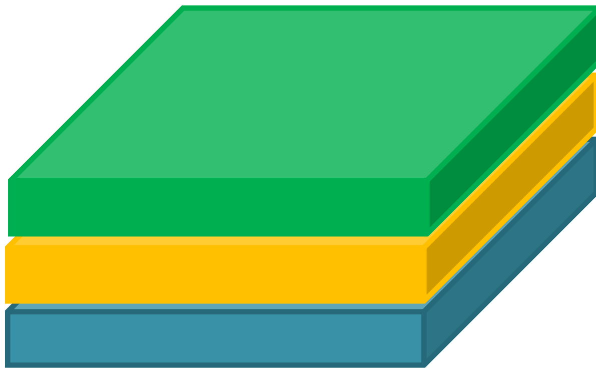


- Other kind of sensors
- Number and location of sensors
- Aggregation of sensor information



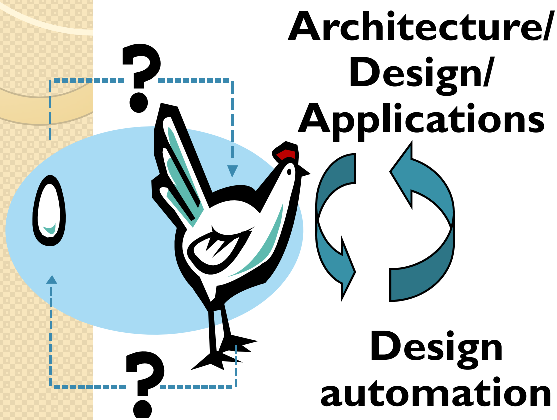
– David Blaauw, UMich

Adding a communication network



- By moving from 2D to 3D have many more close neighbors
- Design space exploration
  - Many TSV's → higher bandwidth → lower yield
  - …
- Other interconnect technologies like RF and optical
  - Interface circuitry issues
  - Thermal issues

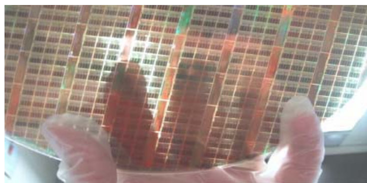
3D challenges



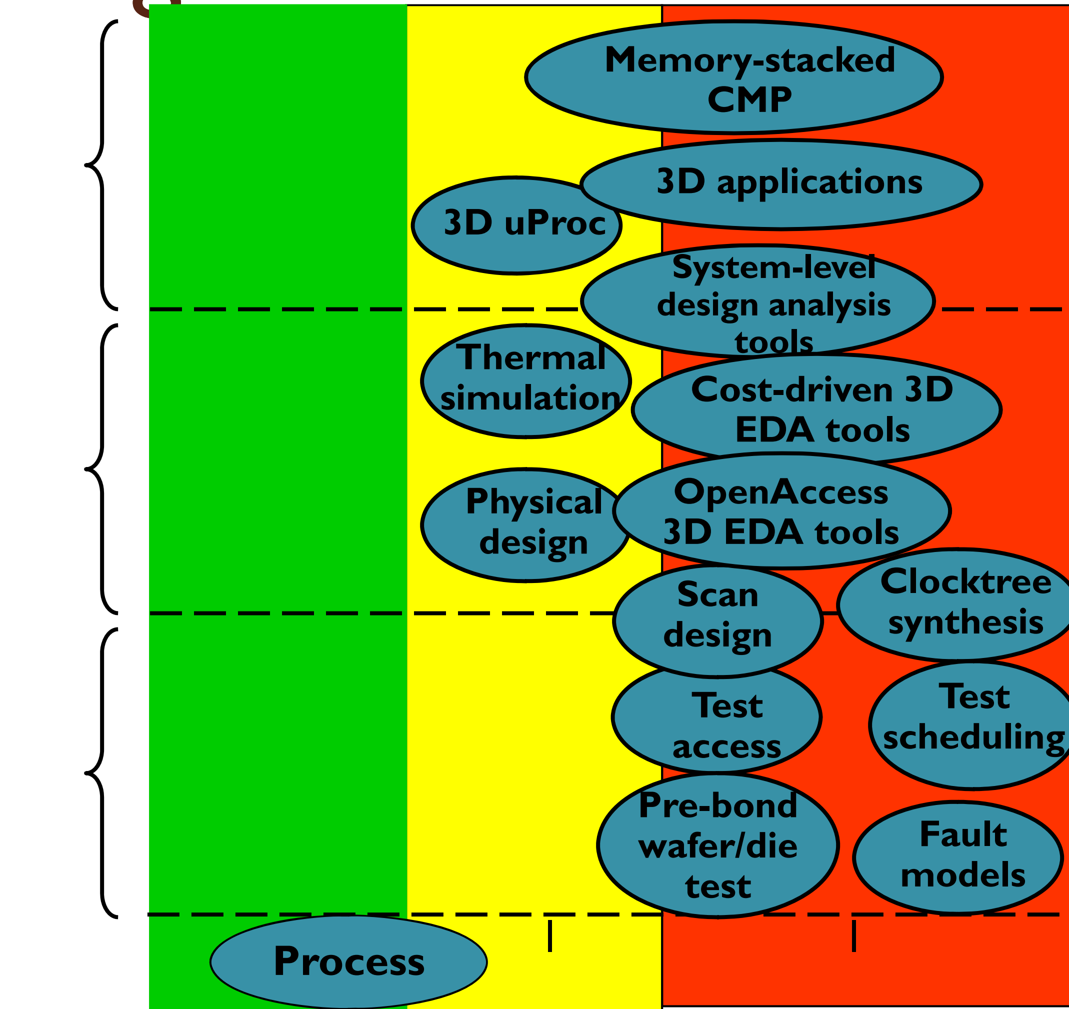
Architecture/ Design/ Applications

Design automation

Testing and design-for-testability



– IBM 11/2002

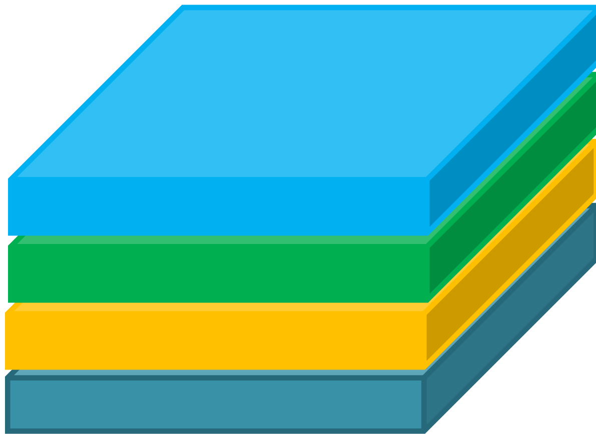


Nearly Mature

Research initiated, Some tools/techniques available

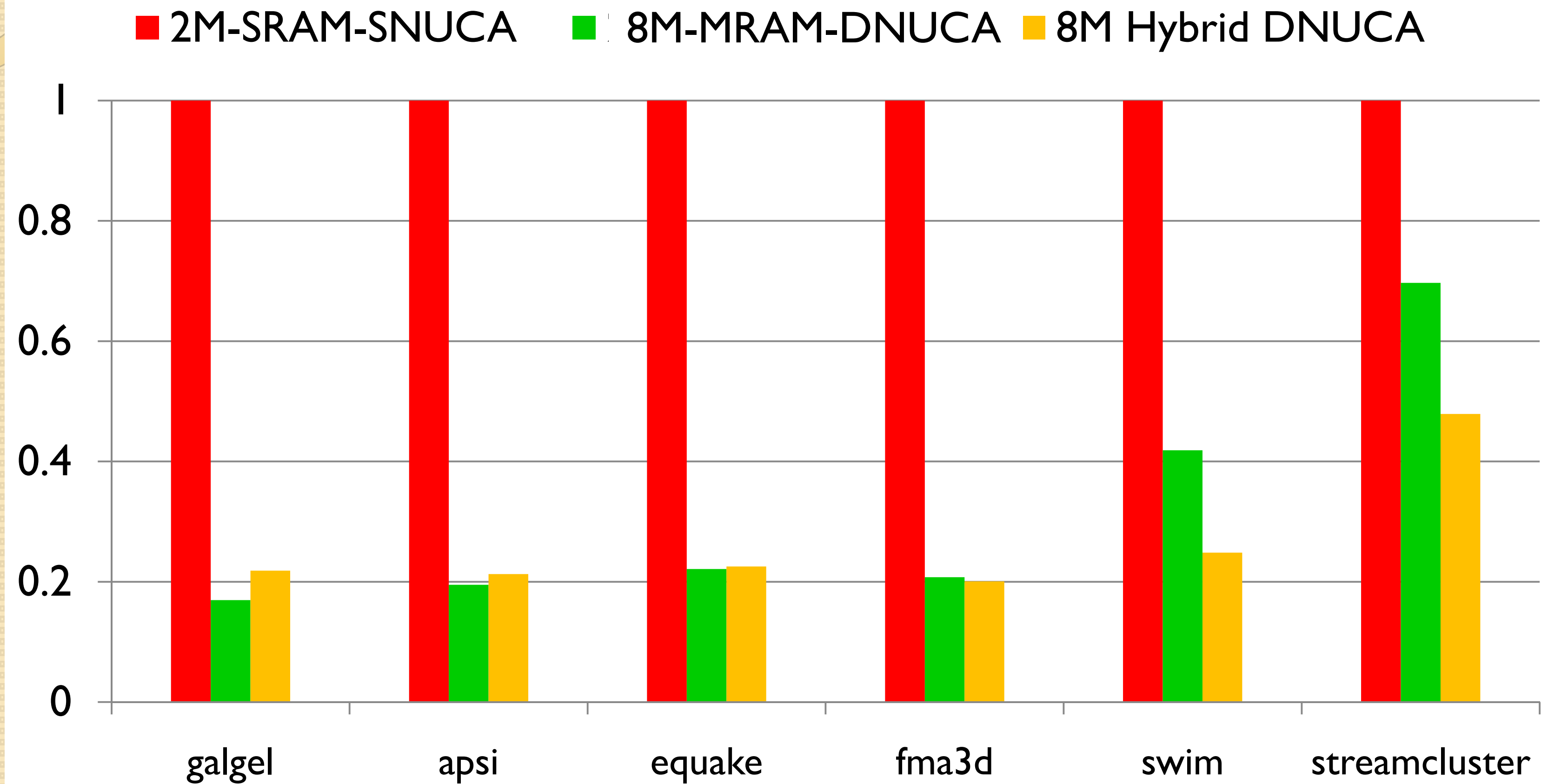
No solutions available, research needed

Adding (nonvolatile) memory



- Use 3D memory stacking to take advantage of the increased bandwidth and reduced latency
- Will probably require a redesign of the memory organization/interface
- Stacking NVM (MRAM, PCRAM, …)
  - Instant on/off, rad hardened
  - Extremely low leakage
  - Long write latencies and large write energy

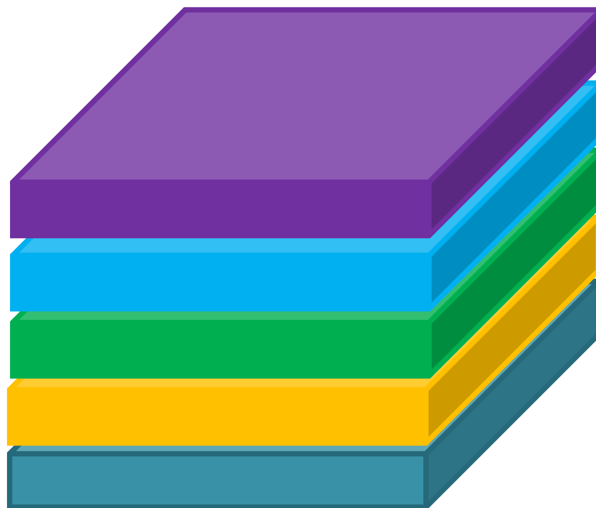
MRAM (L2 cache) stacking



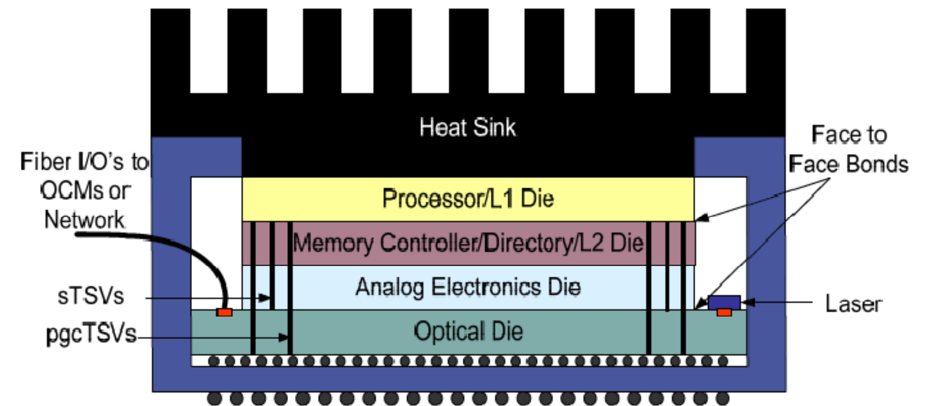
Total Power Comparison

– Yuan Xie, PSU

Adding I/O



- "Traditional" I/O with optical device stacking



– HP Labs, ISCA 08

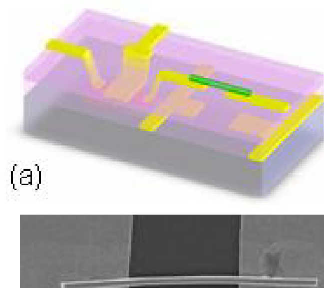
- Nontraditional I/O

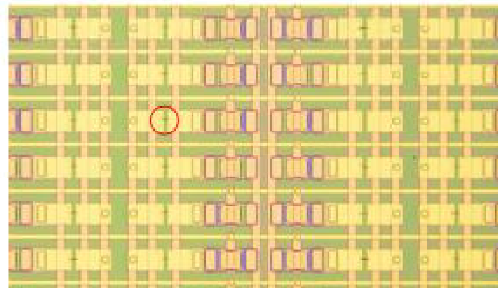
Nontraditional I/O

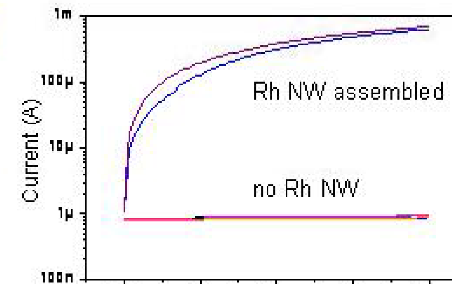
- Chemical sensors
  - Electrofluidic nanowire and nanobead self assembly

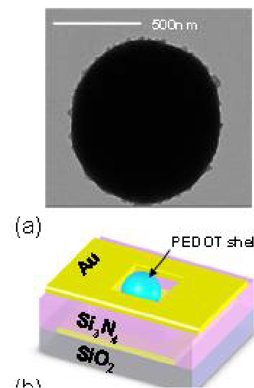
– Tom Mallouk, Chemistry, PSU

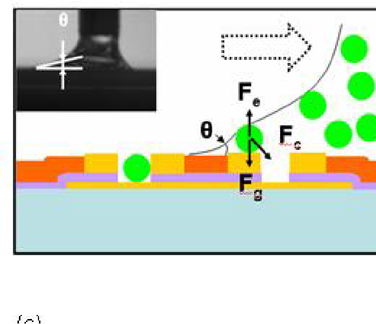
–Theresa Mayer, EE, PSU

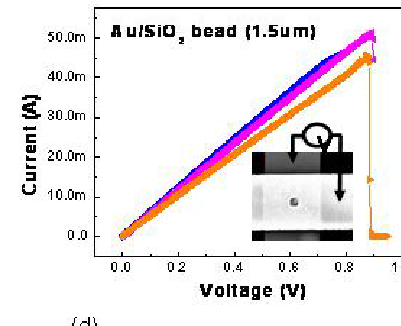




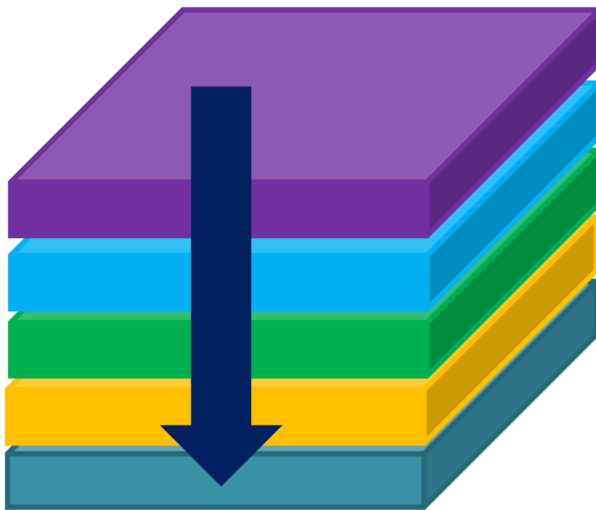






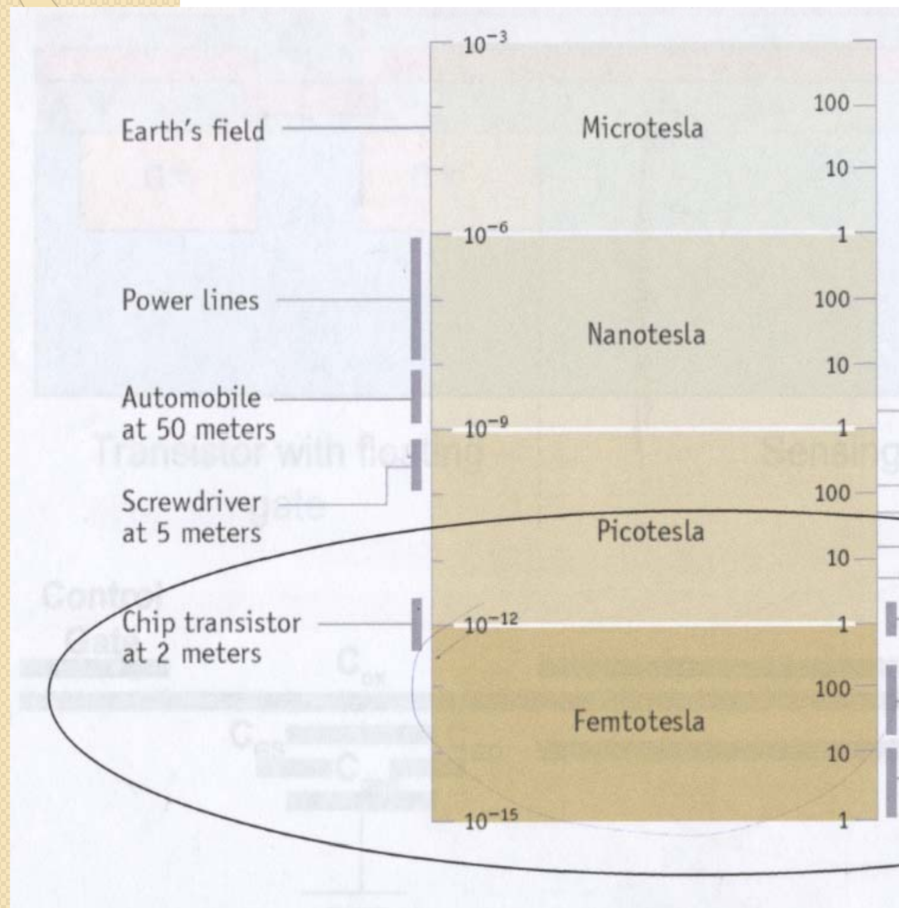


A nano nose application



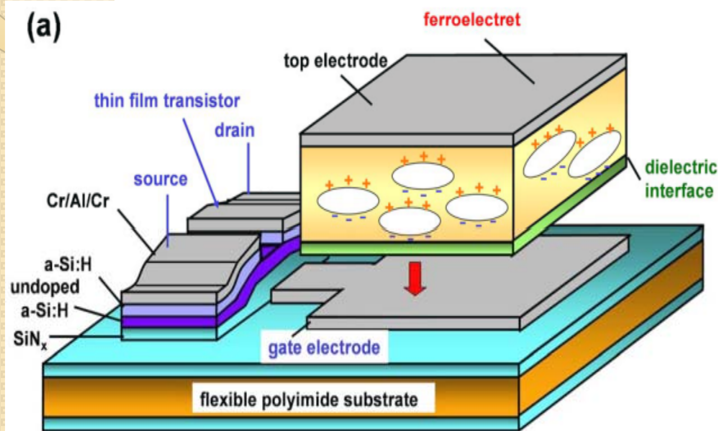
- Input – digitized responses from (100x100) gas sensor array
- Memory – threshold value storage
- Compute fabric – neighborhood aggregation (e.g., systolic array)

More nontraditional I/O



- Biomedical imaging
  - Measure *tiny* magnetic fields
- Use magnetoelectric sensors (Magnetic field → Strain → Electric field)
  - Magnetostriction (materials that change their shape in response to a magnetic field)
  - Piezoelectricity (generate electric potential in response to applied mechanical stress)

Integrated sensor transistor



- Low parasitics from elimination of lossy cable
- Very low external noise
- Easy batch fabrication for array demonstration

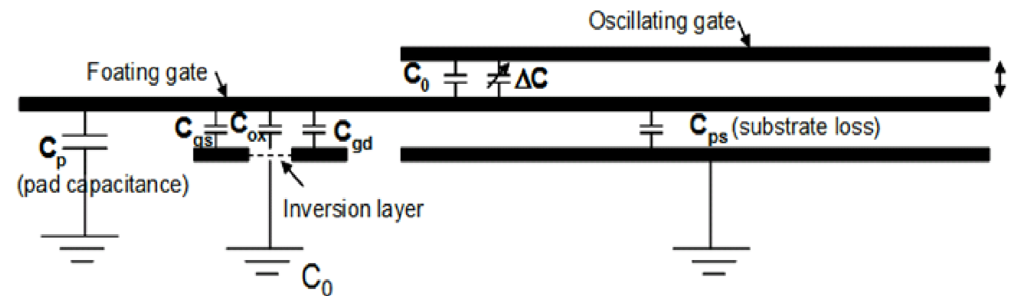


Fig.4a Integrated sensor systems with associated parastics

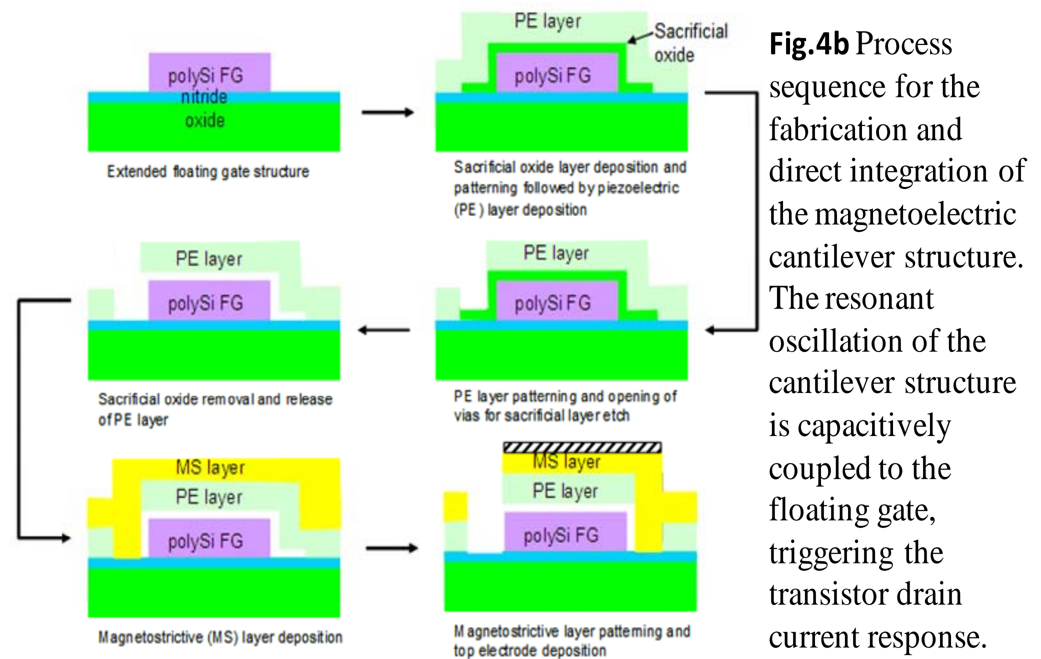
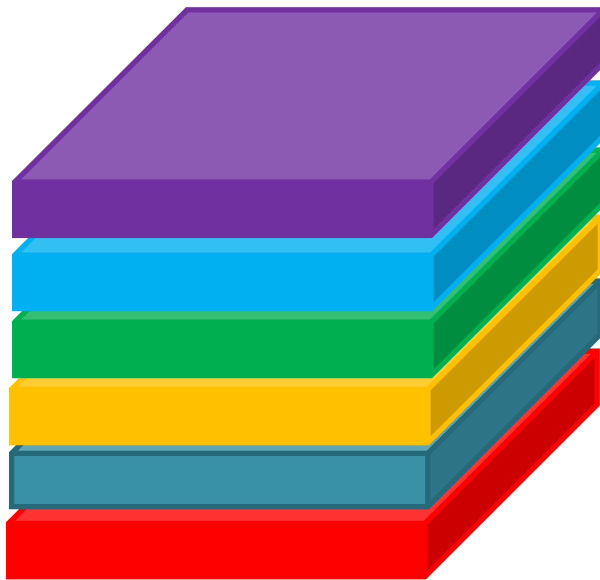


Fig.4b Process sequence for the fabrication and direct integration of the magnetoelectric cantilever structure. The resonant oscillation of the cantilever structure is capacitively coupled to the floating gate, triggering the transistor drain current response.

– Suman Datta, PSU

Adding a power supply



- Energy buffer (battery or capacitor)
  - Recharge issues (especially if the device is implanted)
- Energy scavenging
  - Stray RF sources, vibration, kinetic energy, thermoelectric generators, micro wind turbines, etc. (en.wikipedia.org/wiki/Energy_harvesting)

Material
Scientists/Engr.
Chemists,
Physicists

Designer

Application
Domain
Experts

EDA
Researcher

Device
Physicists /
Fabricators