# IPEM - Interconnect Performance Estimation Model


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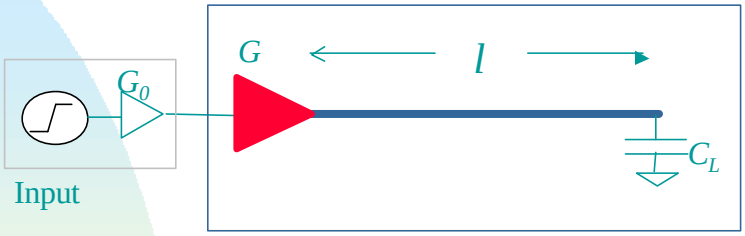
http://cadlab.cs.ucla.edu/software_release/ipem/htdocs/

## Interconnect Layout Optimization

- UCLA Tree-Repeater-Interconnect Opt. (TRIO) Package [Cong et al, ICCAD'97] as an example
  - Interconnect topology optimization
  - Optimal buffer insertion
  - Wiresizing optimization
  - Global interconnect sizing and spacing
  - Simultaneous driver, buffer, and interconnect sizing
  - ……
- Delay can be improved significantly (e.g., 5-10x) !
- Should be considered as early as possible for design convergence. → IPEM

# IPEM Problem Formulation




| | |
|---|---|
| $R_{d0}$ | driver effective resistance of the input stage $G_0$ |
| $R_d$ | driver effective resistance of $G$ |
| $l$ | interconnect wire length |
| $C_L$ | loading capacitance |

**What is the optimized delay/area, …?**
**(without running TRIO or other opt. tools!)**

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# IPEM: *Capabilities and Features*

- **Capabilities (APIs):**
  - OWS (Optimal Wire Sizing)
  - SDWS (Simultaneous Driver and Wire Sizing)
  - BIWS (Buffer Insertion and Wire Sizing)
  - BISWS (Buffer Insertion, Sizing and Wire Sizing)
  - Calculate the critical length for buffer insertion with consideration of wire-sizing optimization
  - Default and user-specified technology parameters.
- **Features:**
  - simple closed-form formulae or computational procedures
  - constant running time in practice (10,000x faster than TRIO)
  - high accuracy (about 90% accuracy on average)
  - IPEM library easily linked to any program/tool

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## Parameters Used in IPEM

- length : length of interconnect, in *mm*.
- Rd : driver resistance, in *ohm*.
- Cl : loading capacitance, in *fF*.
- Rb : buffer resistance, in *ohm*.
- Cb : buffer capacitance, in *fF*.
- tg : intrinsic device delay, in *ps*.
- *k*_max : the max *k*. Driver's size is supposed to be *k* ´ (min gate).
- Rd0 : Effective resistance of the initial driver G0, in *ohm*.
- Rb_array : buffer resistance array, each in *ohm*.
- Cb_array : buffer capacitance array, each in *fF*.
- tg_array : buffer intrinsic delay array, each in *ps*.
- buf_n : number of available buffers available.
- layer_n : layer number.
- gen_n : technology generation number.

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## Example of IPEM under OWS

- Closed-form delay estimation formula

$$T_{ows}(R_d, l, C_L) = \left[ \frac{a_1 l}{W^2(a_2 l)} + \frac{2a_1 l}{W(a_2 l)} + R_d c_f + \sqrt{R_d r c_a c_f l} \right] \cdot l$$

where $a_1 = \frac{1}{4} r c_a$ $a_2 = \frac{1}{2} \sqrt{\frac{r c_a}{R_d C_L}}$

*W(x)* is Lambert's *W* function defined as $we^w = x$

- Closed-form area estimation formula

$$A_{ows}(R_d, l, C_L) = \sqrt{\frac{r(c_f l + 2C_L)}{2R_d c_a}} \cdot l$$

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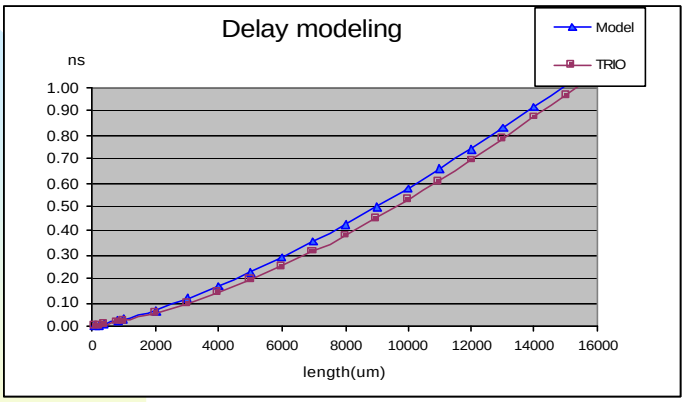
# IPEM vs. TRIO Using OWS




- 0.18um, $R_d = r_g/100$, $C_L = c_g$ x *100*
- For expt., max wire width is 20x min, wire is segmented in every 10um

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# API Example for IPEM

**double**

***Tows* (length, Rd, Cl, layer_n, gen_n)**

**double length, Rd, Cl;**

**int layer_n, gen_n;**

- **Estimate the interconnect delay, under optimal wire sizing.**
- **Return the delay in ps (10^-12 seconds).**

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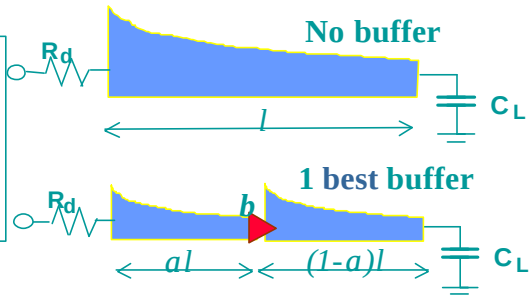
## Critical Length for Buffer Insertion w/ OWS

- Solving critical length $l_{crit}(b, R_d, C_L)$
  - Computed by bisection method
  - Constant time in practice




double

**Lcrit (Rd, Cl, Rb, Cb, tg, layer_n, gen_n)**

double Rd, Cl, Rb, Cb, tg;

int gen_n, layer_n;

- Estimate critical length for buffer insertion under optimal wire sizing.
- Return the critical length, in um.

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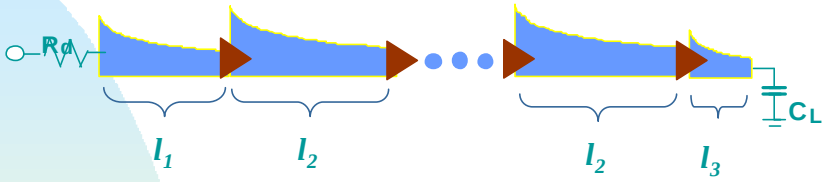
## BIWS & BISWS




- BIWS (Simultaneous Buffer Insertion and Wire Sizing)
  - Insert buffer
  - Optimize wire size
- BISWS (Simultaneous Buffer Insertion, Sizing and Wire Sizing)
  - Insert buffer
  - Optimize buffer size
  - Optimize wire size

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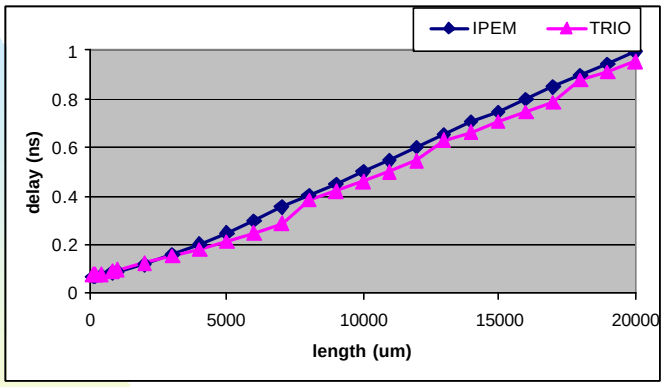
## IPEM vs. TRIO Using BIWS




- *0.18 um, $R_{d0} = r_g/10$, $C_L = c_g$ x 10,* buffer type is 100 x min.
- For expt., max. wire width is 20x min. width, wire is segmented in every 100um.

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## Application of IPEM

- Layout-driven RTL and physical level floorplanning.
- Considering interconnect opt. in logic level synthesis.
  - Use IPEM to predict accurate interconnect delay without really going into layout details
  - Use accurate interconnect delay to guide synthesis
- Interconnect Planning.
- MARCO/GSRC: GTX (Ground Truths/Technology Extrapolation).
- ……

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