Objectives:

- Obtain a general understanding of IC designs.
- Understand the process of VLSI layout design
- Study the basic algorithms used in layout design of VLSI circuits.
- Learn about the physical design automation techniques used in the best-known academic and commercial layout systems.
- Get know hot research topics and problems.
Course Requirements

• Prerequisites
  – CS 180 and CS 51A
  – Consent of instructor

• Grading Policy
  – 30% homeworks
  – 30% midterm
  – 40% class project and term paper

Contact Information

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✉ E.mail: cong@cs.ucla.edu

🔍 My office address: Boelter Hall, 4711
Website for Lecture Notes

- For class attendees only. Please don’t distribute.

Chapter 1
Introduction to VLSI Design
VLSI Design Cycle

- Large number of devices
- Optimization requirements for high performance
- Time-to-market competition
- Cost

VLSI Design Cycle

- System Specification
- Functional Design
- Logic Design
- Circuit Design
- Physical Design
- Design verification
- Fabrication
- Packaging, Testing and Debugging
VLSI Design Cycle

1. System Specification
2. Functional Design
3. Logic Design
4. Circuit Design

X = \((AB\cdot CD)+(A+D)+(A(B+C))\)
Y = \((A(B+C))+AC+D+A(BC+D)\)

VLSI Design Cycle (cont.)

1. Physical Design
2. Fabrication
3. Packaging
Physical Design

Physical design converts a circuit description into a geometric description. This description is used to manufacture a chip. The physical design cycle consists of:

1. Partitioning
2. Floorplanning and Placement
3. Routing
4. Compaction

Physical Design Process

Design Steps:
- Partition & Clustering
- Floorplan & Placement
- Pin Assignment
- Global Routing
- Detailed Routing

Methodology:
- Divide-and-Conquer
Physical Design Cycle

Complexities of Physical Design

- More than 10 million transistor
- Performance driven designs
- Time-to-Market

Design cycle

High performance, high cost
Moore’s Law and NTRS’97

- Moore’s Law
  - The min. transistor feature size decreases by 0.7X every three years (Electronics Magazine, Vol. 38, April 1965)
  - True in the past 30 years!

- 1997 National Technology Roadmap for Semiconductors

<table>
<thead>
<tr>
<th>Technology (um)</th>
<th>0.25</th>
<th>0.18</th>
<th>0.15</th>
<th>0.13</th>
<th>0.10</th>
<th>0.07</th>
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<td>Year</td>
<td>1997</td>
<td>1999</td>
<td>2001</td>
<td>2003</td>
<td>2006</td>
<td>2009</td>
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<td># transistors</td>
<td>11M</td>
<td>21M</td>
<td>40M</td>
<td>76M</td>
<td>200M</td>
<td>520M</td>
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<tr>
<td>On-Chip Clock (MHz)</td>
<td>750</td>
<td>1200</td>
<td>1400</td>
<td>1600</td>
<td>2000</td>
<td>2500</td>
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<tr>
<td>Area (mm²)</td>
<td>300</td>
<td>340</td>
<td>385</td>
<td>430</td>
<td>520</td>
<td>620</td>
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<tr>
<td>Wiring Levels</td>
<td>6</td>
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<td>7</td>
<td>7</td>
<td>7-8</td>
<td>8-9</td>
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</table>

Productivity Gap

Chip Capacity and Designer Productivity

Source: NTRS’97
Design Challenges in Nanometer Technologies

- Interconnect-limited designs
  - Interconnect performance limitation
  - Interconnect modeling complexity
  - Interconnect reliability
  - Impact of new interconnect materials
- High degree of on-chip integration
  - Complexity and productivity
  - Limitation of current design abstraction and hierarchy
  - System on a chip
  - Power barrier

Design Styles

![Diagram showing different design styles: Full custom, Standard Cell, Gate Array, FPGA, with factors such as complexity, performance, size, cost, and market time.]
Full Custom Design Style

Standard Cell Design Style
Gate Array Design Style

FPGA Design Style
Field-Programmable Gate-Arrays (FPGAs)

- Programmable logic
- Programmable interconnects
- Programmable inputs/outputs

Comparisons of Design Styles

<table>
<thead>
<tr>
<th>style</th>
<th>full-custom</th>
<th>standard cell</th>
<th>gate array</th>
<th>FPGA</th>
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</thead>
<tbody>
<tr>
<td>cell size</td>
<td>variable</td>
<td>fixed height *</td>
<td>fixed</td>
<td>fixed</td>
</tr>
<tr>
<td>cell type</td>
<td>variable</td>
<td>variable</td>
<td>fixed</td>
<td>programmable</td>
</tr>
<tr>
<td>cell placement</td>
<td>variable</td>
<td>in row</td>
<td>fixed</td>
<td>fixed</td>
</tr>
<tr>
<td>interconnections</td>
<td>variable</td>
<td>variable</td>
<td>variable</td>
<td>programmable</td>
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</table>

* uneven height cells are also used
Comparisons of Design Styles

<table>
<thead>
<tr>
<th>style</th>
<th>full-custom</th>
<th>standard cell</th>
<th>gate array</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>compact</td>
<td>compact to moderate</td>
<td>moderate</td>
<td>large</td>
</tr>
<tr>
<td>Performance</td>
<td>high</td>
<td>high to moderate</td>
<td>moderate</td>
<td>low</td>
</tr>
<tr>
<td>Fabrication layers</td>
<td>ALL</td>
<td>ALL</td>
<td>routing layers</td>
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</tbody>
</table>

Packaging Styles

Printed Circuit Board (PCB)  Multi-Chip Module (MCM)  Wafer Scale Integration (WSI)

The increasing complexity and density of the semiconductor devices are driving the development of more advanced VLSI packaging and interconnection approaches.
Printed Circuit Board Model

- Large number of layers (150a pitch)
- Larger area
- Low performance
- Low cost

MCM Model

- Up to 36 layers (75a pitch)
- Moderate to small area
- Moderate to high performance
- High cost
- Heat dissipation problems
Wafer Scale Integration

- Small number of layers (VLSI technology - 6a pitch)
- Smallest area
- Significant yield problems
- Very high performance
- Significant heat dissipation problems

Comparisons of Packaging Styles

<table>
<thead>
<tr>
<th>Technology</th>
<th>Figure of Merit (inches/psec. density inches/sq in)</th>
</tr>
</thead>
<tbody>
<tr>
<td>WSI</td>
<td>28.0</td>
</tr>
<tr>
<td>MCM</td>
<td>14.6</td>
</tr>
<tr>
<td>PCB</td>
<td>2.2</td>
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</tbody>
</table>

Merit = propagation speed (inches/psec.) * interconnection density (inches/sq. in).
Interconnect resistance was not considered
History of VLSI Layout Tools

<table>
<thead>
<tr>
<th>Year</th>
<th>Design Tools</th>
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</thead>
<tbody>
<tr>
<td>1950 - 1965</td>
<td>Manual Design</td>
</tr>
<tr>
<td>1965 - 1975</td>
<td>Layout editors, Automatic routers (for PCB), Efficient partitioning algorithm</td>
</tr>
<tr>
<td>1975 - 1985</td>
<td>Automatic placement tools, Well Defined phases of design of circuits, Significant theoretical development in all phases</td>
</tr>
<tr>
<td>1985 – 1995</td>
<td>Performance driven placement and routing tools, Parallel algorithms for physical design, Significant development in underlying graph theory, Combinatorial optimization problems for layout</td>
</tr>
<tr>
<td>1995 – present</td>
<td>Interconnect layout optimization, Interconnect-centric design, physical-logical codesign</td>
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</table>

VLSI CAD Conferences

- ACM IEEE Design Automation Conference (DAC)
- International Conference on Computer Aided Design (ICCAD)
- IEEE International Symposium on Circuits and Systems (ISCAS)
- International Conference on Computer Design (ICCD)
- Design, Automation and Test in Europe, Conference and Exhibition (DATE)
- Asia and South Pacific Design Automation Conference (ASP-DAC)
- International Symposium on Physical Design (ISPD)
VLSI CAD Journals

- IEEE Transactions on CAD of Circuits and systems (T-CAD)
- ACM Trans. on Design Automation of Electronic Systems (TODAES)
- Integration: The VLSI Journal
- IEEE Transactions on Circuits and Systems
- IEEE Trans. on VLSI Systems
- IEEE Trans. on Computers

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VLSI CAD Organization

- ACM SIGDA (Special Interest Group on Design Automation)
- IEEE Circuits and System Society
- Design Automation Technical Committee(DATC) of IEEE Computer Society

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Summary

- Physical design is one of the steps in the VLSI design cycle.
- Physical design is further divided into clustering, partitioning, floorplanning, placement, global and detailed routing, and compaction.
- There are four major design styles -- full custom, standard cell, gate array, and FPGAs.
- There are three alternatives for packaging of chips -- PCB, MCM and WSI.
- Automation reduces cost, increases chip density, reduces time-to-market, and improves performance.
- CAD tools currently lag behind fabrication technology, which is hindering the progress of IC technology.