Outline

- Background
- Workshop organization
- Summary of discussions: challenges and opportunities in giga-scale integration for SOC
  - Physical Design & DSM Effects
  - Synthesis
  - Simulation, Test, and Verification
  - System-level Design, IP Integration, and Design Methodologies
  - Programmable Components, Systems + Software
Exponential Growth of Chip Capacity

- Moore’s Law
  - Min. transistor feature size decreases by 0.7X every three years
  - True for at least 30 years! (first published in April 1965)
- 1997 National Technology Roadmap for Semiconductors

<table>
<thead>
<tr>
<th>Technology (nm)</th>
<th>0.25</th>
<th>0.18</th>
<th>0.15</th>
<th>0.13</th>
<th>0.10</th>
<th>0.07</th>
</tr>
</thead>
<tbody>
<tr>
<td>Year</td>
<td>1997</td>
<td>1999</td>
<td>2001</td>
<td>2003</td>
<td>2006</td>
<td>2009</td>
</tr>
<tr>
<td># transistors</td>
<td>11M</td>
<td>21M</td>
<td>40M</td>
<td>76M</td>
<td>200M</td>
<td>520M</td>
</tr>
<tr>
<td>On-Chip Clock (MHz)</td>
<td>750</td>
<td>1200</td>
<td>1400</td>
<td>1600</td>
<td>2000</td>
<td>2500</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>300</td>
<td>340</td>
<td>385</td>
<td>430</td>
<td>520</td>
<td>620</td>
</tr>
<tr>
<td>Wiring Levels</td>
<td>6</td>
<td>6-7</td>
<td>7</td>
<td>7</td>
<td>7-8</td>
<td>8-9</td>
</tr>
</tbody>
</table>

- Enables system-on-a-chip integration

“Double Exponential” Growth of Design Complexity

- C1: complexity due to exponential increase of chip capacity
  - More devices
  - More power
  - Heterogeneous integration, ……

- C2: complexity due to exponential decrease of feature size
  - Interconnect delay
  - Coupling noise
  - EMI, ……

- Design Complexity ∝ C1 x C2
Productivity Gap

Chip Capacity and Designer Productivity

Source: NTRS'97

Headcount is growing and growing and growing

Moore's Law also applies ...

Logic Transistors/Chip (K)

Transistor/Staff-Month

58%/Yr. Complexity growth rate

21%/Yr. Productivity growth rate

Headcount is growing and growing and growing

Moore's Law also applies ...
Why A Joint Workshop at Taiwan

- Taiwan’s semiconductor industry helped the exponential growth of the industry, esp. development of fabless semiconductor industry in the past ten years
- Future system integration happens on a chip at the foundry, as opposed to on a board at the system house.
  - Fabs play a key role in SOC development
- Taiwan’s semiconductor industry has an invested interest to contribute to the advance of design technologies
  - Productivity gap will prevent fab utilization, and lower ROI

Goals of This Workshop

- Simulate innovations in design technology to enable giga-scale integration for System-On-A-Chip
- “Generating interesting proposals” -- Robert Grafton
  - Identify challenges and prioritize them
  - Identify opportunities for innovations
  - Identify industrial solutions on the horizon
  - Identify problems of long-lasting impact for the research community
- Deliverable -- workshop report
  - Need to have the first draft by the end of the workshop
  - Will be widely distributed
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Workshop Schedule (Wed. 8/25/99)

• Morning
  – 8:30-10:30am: Opening speeches and keynote speech
  – 10:45-12:15pm: Attendee introduction and position statements
• Afternoon
  – 2-5pm: Visit TSMC: presentations, discussions, and fab tour
• Working dinner
  – 6:30-9:30pm: Identify top-10 research problems for SOC designs
Workshop Schedule (Thurs. 8/26/99)

- **Morning**
  - 8:30-10am: Group discussions
  - 10:15 - 11:45am: Group discussions

- **Afternoon**
  - 1-2:30pm: Group discussions and summary
  - 3 - 5pm: Integrating group discussions into the first draft of workshop report

- **Evening**
  - 7:30 - 9:30pm: banquet in Taipei

Workshop Attendees

- 26 people in total
  - 16 from US
  - 10 from Taiwan

- A good mix of experts in both industry and academia
  - 14 from academia
  - 9 from industry
  - 1 from research institute
  - 2 observers from NSF
Groups and Group Coordinators

- Physical Design: Steve Kang
- Synthesis: Jyuo-Min Shyu and Steve Lin
- Testing and verification: Tim Cheng
- System-level designs: Bryan Preas
- Programmable components and systems: Steve Trimberger

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Physical Design and DSM Effects-Challenges
S. Kang, C.K. Koh, P. Lo, M. Pedram

- Timing closure with increasing chip complexity and clock frequency
- Clock signal distribution to meet small skew budget especially at high frequencies (Hz range)
- Consideration of on-chip process variations for physical design, accurate clock skew and timing analysis and optimization
- Crosstalk, signal integrity, clock skews are major concerns-provision of new design methodology/control knobs in early design phase
- Physical design geared for process technology migration with new constraints/design guidelines

Physical Design Challenges (cont’d)

- Minimization of hazards and switched capacitances during physical design phase for power reduction
- Extraction of “proper” parasitics in (global) interconnects and substrate- even for power and ground alone, a big problem
- More effective methodologies for integration of physical design with logic synthesis
- Physical design for multiple Vdd/multiple Vt circuits and systems
Physical Design Challenges (cont’d)

- Mask-making technology aware CAD techniques (maskCAD)
- Accurate and efficient power and noise characterization of cells and IP modules
- Management of inductive parasitics for power/ground busses and IR drops
- Thermal management
- Metallic vs. optical interconnects in view of performance, noise/crosstalk, area; wavelength division multiplexing (WDM) in optoelectronics has become mature

Mixed-signal design- noise shielding, guardbanding, substrate engineering CAD tools; more efficient CAD tools to reduce design efforts for mixed design
- RF circuits- Speed vs. I/O protection as in single-chip radio; efficient CAD tools for layout extraction and simulation
- MEMS, MOEMS- New component models and CAD tools development
- Computationally efficient scalable algorithms for physical design optimization, beyond SA and others
- Integrated and flexible physical design system that reflects realistic operating conditions (temperature variations, statistical variations, etc.)- uniform temperature assumption may hide functional failures during simulation
Physical Design-Opportunities (Cont’d)

• Design of efficient on-chip optical interconnects superior to metallic interconnects in view of timing, signal integrity, chip area, power, etc.
• Powerful and fast gridless router that meets all routing, timing, crosstalk constraints and provides high density
• Better formulation and solution of integrated physical design problems to concurrently address wire sizing, buffer insertion, crosstalk avoidance, timing closure, etc.

Synthesis
(Chen, Lin, Potkonjak, Shen, Shyu)

• Synthesis to Support IP Creation
• Hierarchical Synthesis
• Interaction between Synthesis and Layout
• Analog Synthesis
• Bus/Interface Synthesis
Synthesis to Support IP Creation

- Parameterizable Module Generators
- ASIP (Application-Specific Instruction-set Processor), DSP Functional Macros, Application-Specific Memory Modules, BIST, etc
- Easy to Use including Customization
- Provide Test Vectors
- Complete and Precise Documentation

Hierarchical Synthesis

- Better hierarchical synthesis with area, timing, power constraint
- Support usage of IP
- Support incremental (engineering) change
Layout-Based Synthesis

• Need better estimation of physical design effect
• Planning and budgeting of timing, power, area, … constraints for sub-module synthesis to meet
• In-place optimization (incremental resynthesis)

Analog Synthesis

• Very sensitive to noise
• Need architectural exploration
• Automatically generate simulation, power, layout, … models
• Need to use reduced models for optimization
• Requires interactive synthesis environment
**Bus/Interface Synthesis**

- Protocol specification
- Bus architecture and implementation
- Interconnect physical synthesis
- Performance estimation and evaluation
- Flexible and fast dedicated interface design
- Time-segmented scheduled bus synthesis
- OS & Compiler support

**Advice**

- Don’t try to fully automate everything
- Be domain-specific
- Be evolutionary
- Let designer in control
Test Challenges

- **Exploding volume of test data**
- **Lack of tools for analog/mixed-signal test development**
- **New failure modes for DSM devices**
  - Power bus noise
  - Substrate noise
  - Crosstalk-induced delay faults
  - Distributed delay defects
- **Lack of methodologies for testing heterogenous components in SOC**
- **ATE limitations**
  - Test measurement errors reaching >20% of clock period
  - Increasing yield loss due to ATE inaccuracy
  - Limited capacity and bandwidth and soaring cost of ATE
- **Lack of cost-effective solutions for known good die**
Bandwidth Problems for Test Data Delivery

- Volume of test data per gate is expected to remain constant
- much more data needs to get across the chip boundary, resulting in bandwidth problems.

Max Number I/O Pads for wafer test

Volume of Maximum External Test Vectors (without BIST or DFT)

Test Challenges

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Mixed-Signal Component Design & Test

- Expensive test equipment and long test time
- Lack of tools for analog/mixed-signal test development
  - Mainly functional testing
  - No figure of merits for test program
  - No generally accepted fault model
  - No generic DfT methodology

Test Challenges

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On-chip clock speed increases dramatically while the tester Overall Timing Accuracy (OTA) does not.

Increasing Yield Loss

Source: SIA Roadmap 1997
Paradigm Shifts - Testing

- Higher-level design and test handoff
  - Testability must be analyzed/inserted early in the design process of chips and systems
- Test systems must become simpler
- ICs must be capable of more self test
- ATE will always be required, but its role will change
- Many of today’s DSM design validation problems will become tomorrow’s test problems

Research Opportunity - SOC Testing

- Testing strategy/standard for embedded IP blocks
- Full-chip self-test techniques/methodologies for systems-on-chip
- BIST/BISR for embedded memory
- SOC interface testing
- SOC test scheduling/power control
- SOC test synthesis tool development
**Research Opportunities - Testing DSM, Heterogeneous SOC**

- New fault modeling, analysis and test strategies for deep submicron digital devices
  - Modeling/testing the noise faults in DSM digital devices
- Diagnostic methodologies/tools for DSM devices
  - Shortening process/design debugging times
  - Monitoring manufacturing defects
- Test solutions for analog/mixed signal/RF circuits
  - BIST solutions for analog and analog-digital interface blocks in mixed-signal designs
  - Modeling/DFT/BIST for high frequency (to GHZ range) RF circuits

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**Research Opportunities - Performance/Delay Testing**

- Applying signals on chip with greater accuracy than available at the tester.
- Delay test in multi-clock designs (synchronized or not), including on-chip generated clocks
- Delay testing incorporating interconnect, including coupling capacitance, supply line effects and resistive bridges for many levels of metal
- High speed/frequency test
  - Testing in high speed chips will require attention to:
    - energy consumption during switching
    - careful consideration during ATPG of race conditions
    - multicycle delay paths, etc.
Research Opportunities
- Cost-Effective Solution to Known Good Die

- Bare die quality is crucial to yield and cost of MCM
- Cost-effective at-speed test and burn-in solutions to bare die are not generally available
- Existing solutions are expensive -
  - At-speed test capability at the wafer level using membrane probe technologies
  - Bare-die burn-in using bare-die socket approaches
  - Wafer-level burn-in
  - Incorporation of design-for-testability and built-in self-test strategies for bare-die.

Challenges in Functional Verification

- Verification is increasingly a bottleneck
  - Formal Verification has very limited capacity
  - Simulation/emulation cannot keep up with the demand of SOC
    - Low coverage
    - Emulators remain expensive and hard-to-use
  - Lack of mixed-mode/mixed-level simulation framework for heterogeneous SOC
Functional Verification: Coverage vs. Scale

- Model checking
- FSM-based test generation
- Symbolic simulation
- Manual test w/ coverage
- Random simulation

Scale (gates)

Challenges in Simulating Heterogeneous System-on-a-Chip

Sensor

Sensor

Digital Output

Analog Output

Amp

ADC

Micro-Controller

Comm Interface

Load

Amp

DAC

H-Bridge

Process

Actuator

Motor

Heater

etc.
**Functional Verification**

Coverage vs. Scale

- Model checking
- FSM-based test generation
- Symbolic simulation
- Manual test w/ coverage
- Random simulation
- Hybrid solutions

**Multi-Level/Mixed-Mode/Mixed-Technology Simulation Framework**

- Supports modeling of vastly different functional blocks
- Predicts interference between the blocks
- Simulates whole chip performance accurately within reasonable time
- Includes optimization capability to trade-off among design quality factors such as area, power, signal integrity, and manufacturing yield
System Design Issues

Bryan Preas, Albert Wang, Liang-Gee Chen, Al Dunlop, Massoud Pedram

Outline

- Design Methodology
- Core-based Design
- IP-related Issues
- Architectural Design
- Multi-disciplinary Design
- Productivity
- Orphans
Needs for Implementing Core Based Design Methodology

- Standard protocols and interfaces among blocks
  - Challenge: create a minimal comprehensive set of protocols
- Inter-block communication protocol synthesis
- Reconfigurable interconnection
- Appropriate languages for SOC designs

Core-based Design

- Will have geographically-distributed design teams
- Cores will be used in unexpected ways: must have robust designs (e.g. TCP/IP)
  - Spend transistors to buy design ease
- Stratification of designers
  - Authors vs. composers
- More importance on specification, characterization, standardization, process migration
IP-related Issues

- Export (Core creation)
  - implementation, tool support, documentation, test, customer support, etc.
- Import (Core selection)
  - evaluation, qualification, compatibility, etc.
- IP Protection
  - water mark, finger printing, encryption, etc.
  - customer’s ease of use and verification
- Design reuse cost minimization
  - Version control
    - enhancements, process migration

Architectural Design

Important Topics

- Architectural analysis and exploration
  - Challenge: close the gap between system and RTL levels of design
- System-level partitioning and synthesis
- Design at higher levels of abstraction requires new views: core I/O, behavioral, software, cost, timing, power
- Power source control and management
Multi-disciplinary Design

- HW/SW design
  - Co-specification, co-analysis, co-design and co-verification (co-x)
  - HW/SW mapping and optimization
  - Optimizing software for embedded applications
    - Help software developer
  - High-level power management and control
- Multi-disciplinary optimization including: packaging, mechanical, sensors, acoustical, optical, electrical, software

Productivity

- Move to higher levels of design abstraction
  - Domain-specific design knowledge
- Design reuse
  - Design time tradeoff
  - Challenge: make design reuse easier as first use
- Must capitalize on disparate teams of designers from different geographic locations
Orphans

- System-in-package
- Error detection and recovery
- Fault diagnosis and repair
- Field test and diagnosis

Programmability in SOC

Steve Trimberger, Jason Cong, Al Dunlop, Scott Hauck
What is it?

- Programmable-in-ASIC vs. Pre-Fabricated/Off the Shelf
- Microprocessors, microcontrollers, DSPs, FPGAs
- Resource mixes
  - processor array
  - logic array
  - Heterogeneous (FPGA+CPU+ASIC)

What is new in programmable ASICs?

- Iterative/Incremental methodology
  - like software
  - “self emulation”
- IP Portability - perhaps more portable
  - The ASIC abstraction (or processor abstraction)
- Flexibility of reconfigurable logic used for debugging, test
What is new in Pre-fabricated/OTS?

- Test issues evaporate because fabric is fully tested
- DSM signal integrity issues evaporate because fabric is pre-characterized

Challenges & Opportunities

- Incremental Compilation
  - synthesis
  - mapping
  - P&R
  - Verification
  - Software engineering
- New architectures (perhaps?)
  - Application-specific Architectures for FPGA-in-ASIC
- Must estimate needs - design chip before you know exactly what circuits will be mapped to it
- Multiple targets/partitioning
  - Map tasks to ASIC, CPU, FPGA, etc.
Challenges & Opportunities (Cont.)

• Harnessing defect tolerance and self-repair
  – Yield enhancement
  – Field-programmable “blue wire”
• Software support for programmable resources
  – runtime systems
  – compilers
  – debuggers
• Coupling CPU or FPGA to dedicated logic
  – Interfaces to hardware acceleration
  – Interactions between different resource classes (CPU, FPGA, fixed logic, memory)

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