THE QUEST FOR SYNTHESIS AND LAYOUT TIMING CLOSURE

DAC’2000 Tutorial

Presenters:
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Olivier Coudert - Monterey Design Systems
Anthony Drumm - IBM Corporation, Rochester
Patrick Groeneveld - Magma Design Automation

Tutorial Outline

- Part I: Introduction (Jason Cong)
- Part II: Timing closure today (Tony Drumm)
- Part III: Gain-based synthesis (Patrick Groeneveld)
- Part IV: Physical design closure (Olivier Coudert)
- Part V: New approaches to harness global interconnects (Jason Cong)
Tutorial Schedule

- 09:00am: Introduction (Jason Cong)
- 09:10am: Timing closure today (Tony Drumm)
- 10:40am Break
- 11:00am: Gain-based synthesis - 1 (Patrick Groeneveld)
- 12:00pm: Lunch
- 01:00pm: Gain-based synthesis - 2 (Patrick Groeneveld)
- 01:30pm: Quest of design closure (Olivier Coudert)
- 03:00pm: Break
- 03:20pm: New approaches to harness global interconnects (Jason Cong)
- 04:50pm: Wrap-up and conclusions

Exponential Growth of Chip Capacity

- **Moore’s Law**
  - Min. transistor feature size decreases by 0.7X every three years
  - True for at least 30 years! (first published in April 1965)
- 1997 National Technology Roadmap for Semiconductors

<table>
<thead>
<tr>
<th>Technology (um)</th>
<th>0.25</th>
<th>0.18</th>
<th>0.15</th>
<th>0.13</th>
<th>0.10</th>
<th>0.07</th>
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</thead>
<tbody>
<tr>
<td>Year</td>
<td>1997</td>
<td>1999</td>
<td>2001</td>
<td>2003</td>
<td>2006</td>
<td>2009</td>
</tr>
<tr>
<td># transistors</td>
<td>11M</td>
<td>21M</td>
<td>40M</td>
<td>76M</td>
<td>200M</td>
<td>520M</td>
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<tr>
<td>On-Chip Clock (MHz)</td>
<td>750</td>
<td>1200</td>
<td>1400</td>
<td>1600</td>
<td>2000</td>
<td>2500</td>
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<tr>
<td>Area (mm²)</td>
<td>300</td>
<td>340</td>
<td>385</td>
<td>430</td>
<td>520</td>
<td>620</td>
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<tr>
<td>Wiring Levels</td>
<td>6</td>
<td>6-7</td>
<td>7</td>
<td>7</td>
<td>7-8</td>
<td>8-9</td>
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- Enables system-on-a-chip integration
Productivity Gap
- Where Moore Law May Break

Chip Capacity and Designer Productivity

Source: NTRS97

Approaches to Increase Design Productivity

- Raise level of design abstraction
- Use hierarchical design

Both require synthesis and layout timing closure
Levels of Abstraction in VLSI Design

- **Behavior-level Synthesis**
  - Hardware Description Language

- **Logic-level Synthesis**
  - Boolean Equations/Networks

- **Physical-level Design**
  - Billions of Rectangles

Difficulties in Maintaining High-Level Abstraction & Hierarchical Design

- Interconnect delay far dominates device delay
  - Can no longer design in behavior/functional domain

<table>
<thead>
<tr>
<th>Technology (um)</th>
<th>0.25</th>
<th>0.18</th>
<th>0.15</th>
<th>0.13</th>
<th>0.10</th>
<th>0.07</th>
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</thead>
<tbody>
<tr>
<td>Intrinsic gate delay (ns)</td>
<td></td>
<td></td>
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<tr>
<td>1mm (ns)</td>
<td>0.071</td>
<td>0.051</td>
<td>0.049</td>
<td>0.045</td>
<td>0.039</td>
<td>0.022</td>
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<td>2cm no-opt (ns)</td>
<td>2.589</td>
<td>2.48</td>
<td>2.65</td>
<td>2.62</td>
<td>3.73</td>
<td>4.67</td>
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<td>2cm best-opt (ns)</td>
<td>0.895</td>
<td>0.793</td>
<td>0.77</td>
<td>0.7</td>
<td>0.77</td>
<td>0.672</td>
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</table>

- Best-opt uses simultaneous buffer insertion, driver/buffer sizing, and wiresizing
- Reverse scaling of higher metal layers were not considered
Difficulties in Maintaining High-Level Abstraction & Hierarchical Design

- Current design hierarchy is based on functionality
  - interconnect delay
  - crosstalk
  - P/G bounce due to simultaneous switching, etc …

=> do not fit naturally into function hierarchy

Coupling Noise Problem

Coupling noise from two adjacent aggressors to the middle victim wire (1 mm) with 2x min. spacing. Rise time is 10% of projected clock period.

- Coupling noise depends strongly on both spatial and temporal relations!
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