FPGA’2013 Panel

Are FPGAs Suffering from the Innovator’s Dilemma?

Moderator: Jason Cong, UCLA

Panelists

Jonathan Bachrach, UC Berkeley
Robert Blake, CEO, Achronix
Misha Burich, CTO, Altera
Chuck Thacker, Technical Fellow, Microsoft Research
Steve Trimberger, Fellow, Xilinx
Credit – Idea of the Panel

Jonathan Rose at Univ. of Toronto

Sabbatical in Shanghai, China
FPGA Industry Has Been Innovating and Riding on Moore’s Law

- Oscillator
- Block RAM
- Distributed RAM
- CMOS / TTL Programmable I/O
- Multi-Standard Programmable I/O Support
- Dual Port RAM
- Phase Locked Loops
- LVDS Transceivers
- Multi-Gigabit SerDes
- DSP
- Processor
- PCI Interface
- Ethernet MAC
- Mixed Signal System Monitor
- Phase Multi-Mode Clock Generators
- I/O Termination Impedance
- System Power
- System Performance
- BOM Cost
- System Power
- BOM Cost
- System Performance
- Number of LCs

Year:
- 1985
- 1990
- 1995
- 2000
- 2005
- 2010
- 2015

source: XILINX
### FPGA Has the Highest Margins in Semiconductor

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Gross Margin</th>
<th>Operating Margin</th>
<th>Pre-tax Margin</th>
<th>Net Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMD</td>
<td>22.80%</td>
<td>-17.60%</td>
<td>-22.40%</td>
<td>-21.80%</td>
</tr>
<tr>
<td>ALTR</td>
<td>69.60%</td>
<td>33.20%</td>
<td>33.20%</td>
<td>31.20%</td>
</tr>
<tr>
<td>INTC</td>
<td>62.20%</td>
<td>27.40%</td>
<td>27.90%</td>
<td>20.60%</td>
</tr>
<tr>
<td>MU</td>
<td>11.80%</td>
<td>-7.50%</td>
<td>-12.70%</td>
<td>-12.50%</td>
</tr>
<tr>
<td>NVDA</td>
<td>51.40%</td>
<td>16.20%</td>
<td>16.60%</td>
<td>14.50%</td>
</tr>
<tr>
<td>XLNX</td>
<td>64.90%</td>
<td>28.90%</td>
<td>26.70%</td>
<td>23.70%</td>
</tr>
</tbody>
</table>

Source: Morgan Stanley
So, What’s the Problem?

The FPGA fraction is only $4.5B/$300B = 1.5% of semiconductor industry, and has been that way for 10+ years!

Source WSTS (January 2013) and Xilinx
ASIC Product Segment Marketshare

Source: IC Insights

Year

05 ($16.9B) 11 ($16.4B) 16F ($22.8B)

Marketshare

60% 50% 46%
19% 30% 37%
5% 2% 1%
16% 18% 16%
<1% <1% <1%

Other Full Custom MOS Gate Array MOS PLD MOS Std. Cell
FPGA Market Segment Breakdown

**Altera Market Segment Breakdown (2011)**
- Telecom & Wireless: 43%
- Industrial Automation, Military & Automotive: 17%
- Networking, Computer & Storage: 17%
- Other: 23%

**Xilinx Market Segment Breakdown (2011)**
- Communication: 47%
- Industrial & Other: 32%
- Consumer & Automotive: 15%
- Data Processing: 6%

**Altera Market Segment Breakdown (2003)**
- Communication: 44%
- Industrial: 30%
- Consumer: 15%
- Computer & Storage: 11%

**Xilinx Market Segment Breakdown (2003)**
- Communication: 55%
- Consumer, Industry & Other: 24%
- Storage & Servers: 21%

Source: [www.altera.com](http://www.altera.com) [www.xilinx.com](http://www.xilinx.com)
Are Innovations Driven by Customers?

- Oscillator
- Block RAM
- Distributed RAM
- CMOS / TTL Programmable I/O
- Multi-Standard Programmable I/O Support
- Dual Port RAM
- Phase Locked Loops
- I/O Termination Impedance
- LVDS Transceivers
- Multi-Gigabit SerDes
- Processor
- Ethernet MAC
- PCI Interface
- Mixed Signal System Monitor
- Phase Multi-Mode Clock Generators
- I/O Buffers with Programmable Drive Strength
- CMOS / TTL Programmable I/O
- Stacked Silicon Interconnect
- Agile Mixed Signal Converter
- Extensible Processing Sub-system

Year

Number of LGs
$10^2$, $10^3$, $10^4$, $10^5$, $10^6$, $10^7$
Innovator’s Dilemma

- “There are times at which it is right not to listen to customers, right to invest in developing lower-performance products that promise lower margins, and right to aggressively pursue small, rather than substantial, markets.”

- “Innovator’s dilemma -- “good” companies often begin their descent into failure by aggressively investing in the products and services that their most profitable customers want.”

- “This book addresses a tough problem that most successful companies will face eventually. It’s lucid, analytical – and scary”
  – Andrew S. Grove, chairman & CEO, Intel Corporation
Number of User of Facebook

Number of Facebook Users in Millions

source: www.facebook.com
The Genome Sequencing Revolution

Cost of computing (Moore’s Law)

Cost of Sequencing

Human Genomes Sequenced

$3 billion

$1,000

The Economist

source: Intel
Example of Emerging Technologies: Burrows Wheeler Aligner

- **BWA 0.5.10 workflow**
  - 2 @ aln + sample
  - 8.8x - 9.4x over x86
  - 62 - 67 K Reads/Sec

- **Reference G1k v37**
  - 3.1 G bases

- **Reads**
  - HG00124 SRR189815_(1,2)
  - 242 M reads, ~100 bp
  - 24.7 G bases

![Bar chart showing Reads Per Second for different processors and runs: 7,114 for 12C x86, 25,327 for HC-1, 27,249 for HC-1ex, 62,323 for HC-2, and 66,869 for HC-2ex.](chart.png)
Fine-grain Accelerator Composition + Globally-managed Buffer in NUCA [ISLPED’12]

Example of ABB Flow-Graph (Denoise)

\[
\frac{1}{\sqrt{\sum_{i=0}^{6} (X_i - Y)^2}}
\]

ABB Islands:
- Sharing SPM, DMAC and NoC Interface between multiple ABBs

Accelerator Block Composer
- To orchestrate the data flow between ABBs
- To create a virtual accelerator

Accelerator BiN Manager
- Interval-based buffer allocation
- Buffer fragmentation handling

Experimental results vs ARC
- Workload: Medical imaging
- Denoise, Deblur, Registration, Segmentation
- Speedup over multi-core: Average 158 X (max 359X)

Chuck Thacker, Technical Fellow, Microsoft Research

- BA in physics from U.C. Berkeley in 1967
- Spent 40 years in several industrial research labs, including Xerox PARC, DEC System Research Center, Microsoft
- Long list of awards
  - ACM's Software Systems Award for the development of the Alto (with B. Lampson and R. Taylor)
  - IEEE member, ACM fellow, the American Academy of Arts and Sciences member, the National Academy of Engineering member.
  - In 2004, the Charles Stark Draper prize (with A. Kay, B Lampson, and R. Taylor).
  - IEEE John Von Neumann medal
  - ACM Alan Turing Award (2010)
Jonathan Bachrach, UC Berkeley

- BS degree from the University of California at San Diego and MS and PhD degrees from the University of Massachusetts at Amherst.
- Research areas: spatial, parallel and unconventional programming languages, computing and robotics.
- Cofounded Other Lab where he researched programmable matter and geometry workflows for fabrication.
- Research scientist at MIT for 8 years, held postdocs at Stanford and ICSI, and was a researcher at IRCAM in Paris, developing new musical platforms.
Robert Blake, CEO, Achronix

- MEng. in Business and Microelectronics and BSc. in Applied Physics & Electronics from the University of Durham in England.
- 25 years of experience in the semiconductor industry.
  - CEO of Octasic Semiconductor based in Montreal, Canada.
  - Vice President of Product Planning at Altera: responsible for defining Altera’s programmable logic product solutions. He has been developing ASIC and programmable logic for high speed telecom and network applications for over 17 years.
  - Prior to Altera, worked at LSI Logic and Fairchild where he developed ASIC technology.
Misha Burich, CTO, Altera

- Ph.D. and M.S. in Electrical Engineering from the University of Minnesota in Minneapolis, and his Dipl. Eng. in EE from the University of Belgrade.
- Began his career at Bell Laboratories Research, Murray Hill in 1978.
- Prior his current role (CTO) at Altera, he was the Senior VP of R&D, managing the whole research and development organization, responsible for all software, IP, system solutions and semiconductor products.
Steve Trimberger, Fellow, Xilinx

- Xilinx Fellow heading the Circuits and Architectures Group in Xilinx Research Labs in San Jose, California.
- Designed the bitstream security functions employed by Xilinx FPGAs and his research led to the development of the Xilinx 2.5D Stacked Silicon Technology.
- Has 200 patents in IC design, FPGA and ASIC architecture, CAE and cryptography.
- He is a Fellow of the ACM and a Fellow of the IEEE.
- Has twice been Program Chair and General Chair of the FPGA Symposium.
Questions to the Panelists

- Is that pressure or desire of keeping the high margin preventing the FPGA industry in breaking into some lower margin market?
- Are the innovations from the FPGA industry mainly driven by the existing customer base, at the expense ignoring other emerging needs?
- Why the FPGA industry is stuck with about 1-2% market share of the semi industry?
- Are there emerging application domains that can be served by the FPGA industry, but not currently, due to the concerns of margin, market size, etc?
- Are there new technologies that the FPGA industry can leverage to break into new market segments?
- What happens when Moore's Law slows down or stops? What new innovation is needed and how will the FPGA industry dynamics change?