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## Kirill Minkovich

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Objective	To get a research position in algorithm development.		
Education	2004 – 2/2010	UCLA, Los Angeles, CA	
	Ph.D. degree in Computer Science <b>Thesis Title: Logic Synthesis for Nanometer IC Technologies</b> <b>Advisor: Jason Cong</b>		
Education	2001 – 2004	UC Berkeley, Berkeley, CA	
	B.A. degree in Computer Science - Overall GPA: 3.72 - Completed December 2003 with Distinction In General Scholarship One class away from B.A. in Math		
Skills	Excellent C programming skills, good knowledge of Perl and C++, knowledge of interrupt handlers, knowledge of popular compilers, have programmed for Windows, Solaris, Linux, uClinux, ability to read and understand schematics, fluent in English and Russian. I have used the following languages in the past: Python, Java, Verilog, Scheme, SQL, x86 assembly, and MIPS assembly.		
Summary of qualifications	9/04-Present	UCLA CADLab	Los Angeles, CA
	Researcher Currently working with Professor Jason Cong ( <a href="http://cadlab.cs.ucla.edu/~cong/">http://cadlab.cs.ucla.edu/~cong/</a> ) in the field of Logic Synthesis. My research can be broken down into four parts:		
	1. Evaluated the scalability and quality of current logic synthesis algorithms by creating difficult benchmarks with known optimal solutions.		
	2. Improved the performance of Boolean matching for technology mapping and showed that cut selection algorithms did not have much room for improvement in terms of area.		
	3. Created a suite of tools for optimizing logic for average-case delay (instead of worst-case delay) which can be used with most timing speculative architectures.		
4. Created a technology mapping algorithm which increase the probability that an FPGA bitstream will function correctly when implemented on a faulty FPGA.			
All four of these parts had a software release which is referenced in the respective publications.			
	6/06-9/06	Altera	San Jose, CA
Researcher (Internship) Figured out how to adapt and change an academic algorithm to fit into their design flow. The new additions provided a 5% area improvement and a 2% delay improvement for their Cyclone family of FPGAs.			
	6/04-10/04	CRC Inc.	Santa Clara, CA
Software Developer (Internship) Developed and implemented a Protocol (over TCP/IP) for communication with a spectrometer running uClinux. Was responsible for writing a complete multi-client server in C and a fully functional client in Visual Basic.			
	5/03-10/03	MKS Instruments	Santa Clara, CA
Software Developer (Internship) Designed an algorithm for detection of their product's state change. Hardware layer application design and development. Created networking programs for UNIX and Windows systems.			

Publications

(**bold** designates primary author)

J. Cong and **K. Minkovich**, "Optimality Study of Logic Synthesis for LUT-Based FPGAs," *Proceedings of the 14th ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, CA, February 2006.

News Articles about paper:

Cover story in EE Times (2/20/06)

FPGA Journal article (4/25/06)

J. Cong and **K. Minkovich**, "Optimality Study of Logic Synthesis for LUT-Based FPGAs," TCAD: Special Edition for FPGA, 2006.

J. Cong and **K. Minkovich**, "A Improved SAT-Based Boolean Matching Using Implicants for LUT-Based FPGAs," *Proceedings of the 15th ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, CA, February 2007.

J. Cong and **K. Minkovich**, "Mapping for Better Than Worst-Case Delays In LUT-Based FPGA Designs," *Proceedings of the 16th ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, CA, February 2008.

J. Cong and **K. Minkovich**, "Logic Synthesis for Better Than Worst-case Designs," *International Symposium on VLSI Design, Automation and Test*, Hsinchu, Taiwan, April 2009.

J. Cong, K. Gururaj, W. Jiang, B. Liu, K. Minkovich, **B. Yuan** and Y. Zou, "Accelerating Monte-Carlo based SSTA using FPGAs," *Proceedings of the 18th ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, CA, February 2010 (to appear).

J. Cong and **K. Minkovich**, "Logic Synthesis for Better Than Worst-case Architectures," under review.

J. Cong and **K. Minkovich**, "LUT-Based FPGA Technology Mapping for Reliability," under review.