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Kirill Minkovich

Objective	To get a research position in algorithm development.		
Education	2004 – December 2009	UCLA, Los Angeles, CA	
	Ph.D. degree in Computer Science - Currently ongoing		
Education	2001 – 2004	UC Berkeley, Berkeley, CA	
	B.A. degree in Computer Science - Overall GPA: 3.72 - Completed December 2003 with Distinction In General Scholarship One class away from B.A. in Math		
Skills	Excellent C programming skills, good knowledge of Perl and C++, knowledge of interrupt handlers, knowledge of popular compilers, have programmed for XP, Solaris, Linux, uClinux, ability to read and understand schematics, fluent in English and Russian. I have used the following languages in the past: Python, Java, Verilog, Scheme, SQL, x86 assembly, and MIPS assembly.		
Summary of qualifications	2/05-Present	UCLA CADLab	Los Angeles, CA
	Researcher Currently working with Professor Cong (http://cadlab.cs.ucla.edu/~cong/) in the field of Logic Synthesis for FPGAs. This work focuses on creating graph based algorithms to optimize large networks of gates.		
	6/06-9/06 (Summer)	Altera	San Jose, CA
	Researcher Figured out how to adapt and change an academic algorithm to fit into their design flow. The new additions provided a 5% area improvement and a 2% delay improvement for their Cyclone family of FPGAs.		
	6/04-10/04 (Summer)	CRC Inc.	Santa Clara, CA
Software Developer Developed and implemented a Protocol (over TCP/IP) for communication with a spectrometer running uClinux. Was responsible for writing a complete multi-client server in C and a fully functional client in Visual Basic.			
Summary of qualifications	11/03-02/04	UC Berkeley	Berkeley, CA
	Algorithm Developer Working with fellow student to design an algorithm that would compare 2 versions of the same DNA, chromosome by chromosome, and create a mapping between the different versions.		
Summary of qualifications	5/03-10/03 (Summer)	MKS Instruments	Santa Clara, CA
	Software Developer Designed an algorithm for detection of their product's state change. Hardware layer application design and development. Created networking programs for UNIX and Windows systems.		

5/02 – 9/02 (Summer) Applied Materials Santa Clara, CA
Software Developer
Developed Automated Test Capabilities.
Developed scenarios where the product might fail.
This software is currently in being used to test their system before being shipped out.

4/99 – 6/01 TeNTA Technologies Santa Clara, CA
Software Developer
Designed and made prototype test fixture for the Gas Panel, CCM, and RCCM.
Developed Software diagnostic Tools for VME based I/O boards.
Created test plans for new hardware and implemented them.

Publications

K. Minkovich and J. Cong, "Optimality Study of Logic Synthesis for LUT-Based FPGAs," *Proceedings of the 14th ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, CA, February 2006.

News Articles about paper:

Cover story in EE Times (2/20/06)

FPGA Journal article (4/25/2006)

K. Minkovich and J. Cong, "Optimality Study of Logic Synthesis for LUT-Based FPGAs," *TCAD: Special Edition for FPGA*, 2006.

K. Minkovich and J. Cong, "A Improved SAT-Based Boolean Matching Using Implicants for LUT-Based FPGAs," *Proceedings of the 15th ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, CA, February 2007.

K. Minkovich and J. Cong, "Mapping for Better Than Worst-Case Delays In LUT-Based FPGA Designs," *Proceedings of the 16th ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, CA, February 2008.

K. Minkovich and J. Cong, "Logic Synthesis for Better Than Worst-case Designs," *International Symposium on VLSI Design, Automation and Test*, Hsinchu, Taiwan, April 2009.

K. Minkovich and J. Cong, "Logic Synthesis for Better Than Worst-case Architectures," under review.

K. Minkovich and J. Cong, "Study of Error Propagation in LUT-base FPGAs," under review.