

# **Interconnect Delay Estimation Models for Synthesis and Design Planning**

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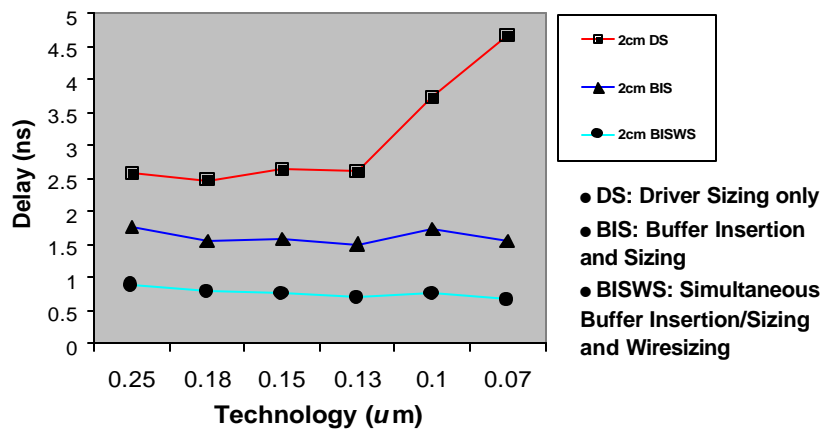
## **Presentation Outline**

- **Introduction & Motivation**
- **Problem Formulation**
- **Interconnect Delay Estimation Models under  
Various Layout Optimizations**
- **Application and Conclusion**

## Impact of Interconnect Layout Optimization

- E.g., UCLA **T**ree-**R**epeater-**I**nterconnect **O**pt. (**TRIO**) Package [Cong et al, ICCAD'97]
  - Interconnect topology optimization
  - Optimal buffer insertion
  - Wiresizing optimization
  - Global interconnect sizing and spacing
  - Simultaneous driver, buffer, and interconnect sizing
  - .....
- Delay can be improved by up to 7x !

## Impact of Interconnect Optimization on Future Technology Generations



## Complexity of Existing Interconnect Opt. Algorithms

- 2cm line, W=20, B=10, segment every 500um
- Use best available algorithms:
  - Local Refinement (**LR**)
  - Dynamic Programming (**DP**)
  - Hybrid of **DP+LR**

	<b>LR</b>	<b>DP+LR</b>	<b>DP</b>	
Algorithm	OWS	BI+OWS	BIWS	BISWS
Delay (ns)	4.5	1.6	1.02	0.81
CPU (s)	0.06	0.42	4.5	12.4

( HSPICE needs additional 60 seconds! )

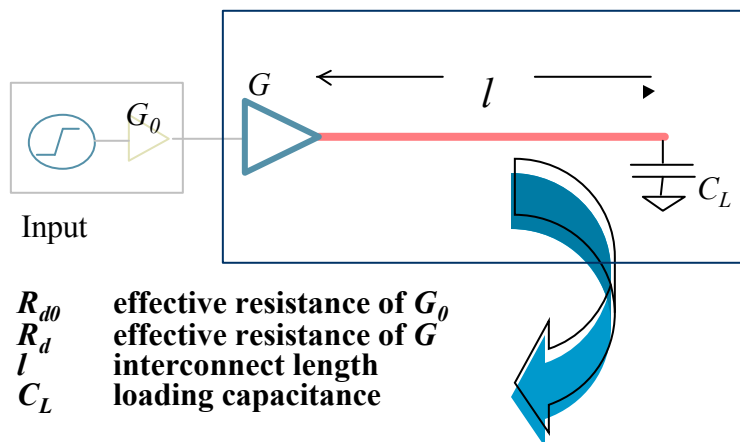
## Needs for Efficient Interconnect Estimation Models

- **Efficiency**
- **Abstraction** to hide detailed design information
  - granularity of wire segmentation
  - number of wire widths, buffer sizes, ...
- **Explicit relation** to enable optimal design decision at high levels
- **Ease of interaction** with logic/high level synthesis tools

## Our Contributions

- Develop a set of **delay estimation models (DEM)** under different **layout optimizations**:
  - **Optimal Wire Sizing (OWS)**
  - **Simultaneous Driver and Wire Sizing (SDWS)**
  - **Simultaneous Buffer Insertion and Wire Sizing (BIWS)**
  - **Simultaneous Buffer Insertion/Sizing and Wire Sizing (BISWS)**
- Our DEM's have
  - closed-form formula or simple characteristic equations
  - constant running time in practice
  - high accuracy (about 90% accuracy on average)

## Problem Formulation



➔ **What is the optimized delay?  
(without running TRIO or other opt. tools!)**

## Parameters and Notations

- Based on 1997 National Technology Roadmap for Semiconductors (NTRS'97)

- **Interconnect**

- $c_a$  area capacitance coefficient
- $c_f$  fringing capacitance coefficient
- $r$  sheet resistance

- **Device**

- $t_g$  intrinsic gate delay
- $c_g$  input capacitance of the minimum gate
- $r_g$  output resistance of the minimum gate

## DEM under OWS

- We obtain **closed-form** delay estimation formula

$$T_{ows}(R_d, l, C_L) = \left[ \frac{a_1 l}{W^2(a_2 l)} + \frac{2a_1 l}{W(a_2 l)} + R_d c_f + \sqrt{R_d r c_a c_f l} \right] \cdot l$$

where

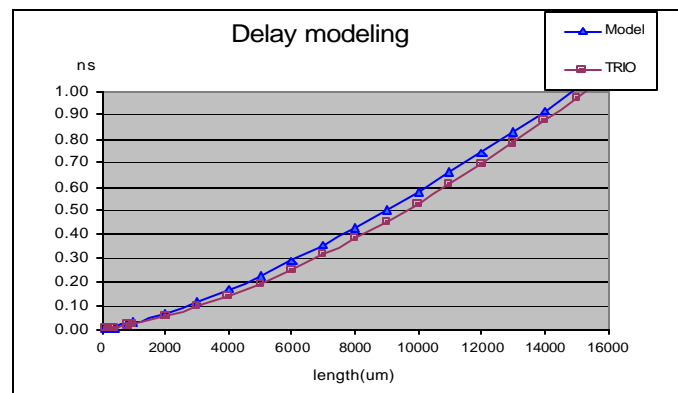
$$a_1 = \frac{1}{4} r c_a \quad a_2 = \frac{1}{2} \sqrt{\frac{r c_a}{R_d C_L}}$$

$W(x)$  is Lambert's  $W$  function defined as  $we^w = x$

## Property of DEM-OWS

- **Theorem:**  $T_{ows}$  is a sub-quadratic, convex function of length  $l$
- **Note:** Without wire-sizing, delay  $\propto l^2$ , as used by most layout-driven logic synthesis systems:
  - Ramachandran et al., ICCAD-92
  - .....
- **Closed-form DEM-OWS will serve as a basis for deriving SDWS, BIWS and BISWS**

## Comparison of DEM-OWS vs. TRIO



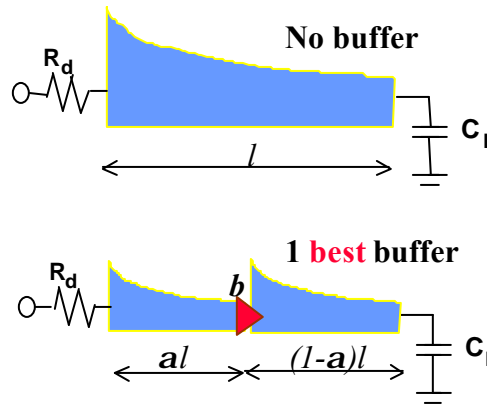
- $0.18\mu\text{m}$ ,  $R_d = r_g/100$ ,  $C_L = c_g \times 100$
- For expt., max wire width is 20x min, wire is segmented in every 10um

## Critical Length for BI under OWS

$$T_{ows}(R_d, l, C_L)$$

Solve for  $l$ , =>  
critical length  
 $l_{crit}(b, R_d, C_L)$

- Computed by bisection method
- Constant time in practice



$$T_{1bws}(R_d, l, C_L) = \min_{0 \leq a \leq 1} \{T_{ows}(R_d, a l, C_b) + t_g + T_{ows}(R_b, (1-a)l, C_L)\}$$

## Critical Lengths $l_{crit}(b, R_b, C_b)$

Decrease

Technology ( $\mu\text{m}$ )	0.25	0.18	0.15	0.13	0.10	0.07
b=10x	4.12	3.80	3.97	3.61	2.92	2.08
b=50x	6.40	5.81	6.01	5.51	4.45	3.30
b=100x	7.47	6.83	7.04	6.39	5.30	3.91
b=200x	8.65	7.92	8.14	7.43	6.35	4.49
b=500x	9.98	9.10	9.30	8.57	7.13	5.21

unit: mm

Min. WS	2.52	2.23	2.14	1.94	1.50	1.43
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- Cf. [Ottens ISPD'98, Ottens-Brayton DAC'98]  
(uniform wire width)

- Denote  $l_c = l_{crit}(b, R_b, C_b)$

## “Logic Volume” within $l_c$

- Defined as the number of min 2-input NAND gates that can be packed within the area of  $l_c/2 * l_c/2$

Technology (um)	0.25	0.18	0.15	0.13	0.10	0.07
2-NAND (um <sup>2</sup> )	7.80	4.04	3.00	2.18	1.28	0.64
b=10x	0.55	0.89	1.31	1.49	1.66	1.69
b=50x	1.31	2.09	3.01	3.48	3.87	4.25
b=100x	1.79	2.88	4.13	4.68	5.48	5.97
b=200x	2.4	3.88	5.52	6.33	7.87	7.88
b=500x	3.19	5.12	7.21	8.42	9.93	10.6

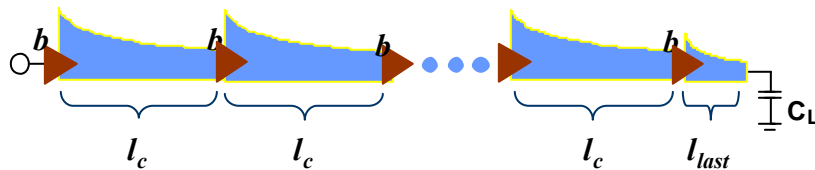
unit: million

→ Increase



## Property of BIWS

- **Theorem:** For BIWS, the distances between adjacent buffers are the same, and equal to  $l_c$  – the critical length.
- **Proof:** based on the convexity of  $T_{ows}$



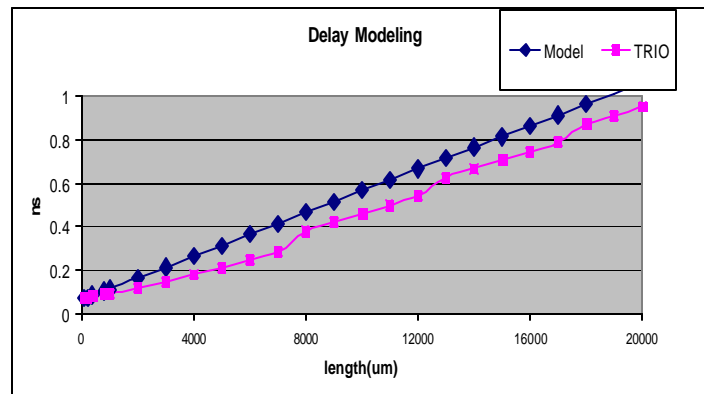
## Linear DEM for BIWS

- Original long interconnect is divided into  $l/l_c$  stages
- The stage number is proportional to  $l$
- Each stage of length  $l_c$  has delay  $T_{ows}(R_b, l_c, C_b)$
- ➔ Linear DEM for BIWS

$$T_{biws} = t_{biws} \cdot l + t_g$$

$t_{biws}$  is the slope, and can be obtained from  $T_{ows}(R_b, l_c, C_b)$

## Comparison of DEM-BIWS vs. TRIO

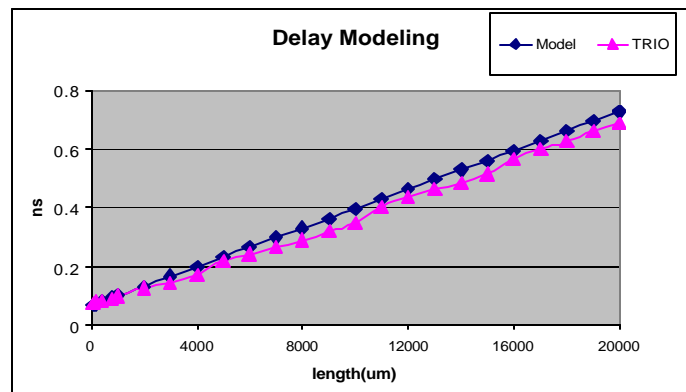


- 0.18 um,  $R_{d0} = r_g/10$ ,  $C_L = c_g \times 10$ , buffer type is 100 x min.
- For expt., max. wire width is 20x min. width, wire is segmented in every 100um.

## DEM under BISWS

- Observations from extensive experiments:
  - Linear delay versus length
  - Internal buffers are about the same size
- Therefore, we estimate BISWS by the best BIWS from available buffer types
- Linear delay model for optimal BISWS
$$T_{bisws} = t_{bisws} \cdot l + t_g$$
where  $t_{bisws} = \min_{b \in B} t_{biws}$ ,  $B$  is the buffer set
- Complexity  $O(|B|)$ . Since the set  $B$  is normally less than 20, constant time in practice.

## Comparison of DEM-BISWS vs. TRIO



- $0.18\mu m, R_{d0} = r_g / 10, C_L = c_g \times 10$
- For expt., max. allowable buffer/driver size is 400x min device; max. wire width is 20x min. width; wire is segmented in every 100um.

## Some Applications of DEM's

- **Layout-driven** RTL and physical level floorplanning
- **Consider interconnect opt. during logic/high level synthesis**
  - Use **DEM** to **predict accurate interconnect delay without really going into layout details**
  - Use **accurate interconnect delay to guide synthesis**
- **Interconnect Planning**
- .....

## Conclusion

- **DEM's with closed-form formula or simple characteristic equations for various interconnect optimization techniques**
  - **Very accurate** (about 90% accuracy on average)
  - **Very efficient** (constant running time in practice)
  - **High level abstraction**
  - **Very easy to be embedded** into any synthesis and planning tools
- **Ongoing work:**
  - **Multiple-pin nets with tree topology (TAU'99)**
  - **Area/Delay trade-off**