

Yi Zou

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Education

- **Tsinghua University Beijing, P.R. China** 09/2000 - 07/2004
(Honored) Bachelor in Computer Science.
- **Tsinghua University Beijing, P.R. China** 09/2004 - 07/2006
(Honored) Master in Computer Science Advisor: Qiang Zhou, Associate Professor, Computer Science Dept.
- **University of California, Los Angeles GPA 3.93/4** 08/2006 – present
PhD Candidate in Computer Science Advisor: Jason Cong, Professor in Computer Science Dept

Research Interest

- Reconfigurable computing, GPGPU, High performance computing
- High-level synthesis and Architecture Templates for FPGAs
- Numerical algorithms and optimizations

Professional Experience

- Research Assistant, Computer Science Dept of Tsinghua Univ 01/2004-07/2006
- Research Assistant, Computer Science Dept of UCLA. 09/2006-present
- Reviewer for FPGA, FPL, SASP, ISLPED, IEEE TVLSI, ACM TODAES, ACM TRETs

Computer Skills

- Extensive experience with C/C++ and VHDL/Verilog
- Development experience on NVIDIA GPUs with CUDA toolkit
- Development experience on Altera and Xilinx FPGAs with Quartus II and ISE/EDK
- Development experience on Linux, Windows, with gcc and Visual C++

Research Projects

- FPGA/GPU accelerator design for lithographic simulations 10/2006-07/2007
- FPGA/GPU accelerator design for capacitance extractions 10/2007-05/2008
- FPGA/GPU-accelerated medical imaging 10/2008-present
- GPU-accelerated circuit placement 03/2009-07/2009
- Task-level synthesis for FPGAs 06/2010-present

Awards

- Honored bachelor graduate of Tsinghua Univ
- Outstanding master graduate of Tsinghua Univ
- SIGDA's CADathlon at ICCAD 2010, First place winner team (with B. Liu)

Working Experience

- FPGA implementation for MPEG4 using C-to-RTL tools AutoPilot
AutoESL Design Technologies 06/2008/-10/2008

- System-level prototyping for web search acceleration

Microsoft Research Asia

06/2009/-09/2009

Publications (in UCLA)

(Note: papers from Prof Cong's group are listed in alphabetic order, bolded papers are those I am the corresponding author)

Journals

- **J. Cong and Y. Zou, "FPGA-Based Hardware Acceleration of Lithographic Aerial Image Simulation", ACM Transactions on Reconfigurable Technology and Systems, Vol.2, No.3, Article 17, 2009**
- J. Cong, W. Jiang, B. Liu and Y. Zou, "Automatic Memory Partitioning and Scheduling for Throughput and Power Optimization," ACM Transactions on Design Automation of Electronic Systems, Volume 16, Number 2, Article 15, March 2011.

Magazines

- Y. Hu, Y-T Wang, A.Stoelting, Y. Zou and M. Sarrafzadeh, "Providing a cushion for wireless healthcare application development", IEEE Potentials Magazine, Vol 29, No. 1, 2010.

Conferences and Workshops

- **J. Cong and Y. Zou, "Lithographic Aerial Image Simulation with FPGA-Based Hardware Acceleration", in Proc. FPGA, pages 20-29, Monterey CA, Feb 2008**
- **J. Cong, K. Gururaj, B. Liu, C. Liu, Z. Zhang, S. Zhou and Y. Zou, "Evaluation of Static Analysis Techniques for Fixed-Point Precision Optimization", in Proc. FCCM 2009, pages 231-234, Napa CA, Apr 2009**
- **J. Cong and Y. Zou, "Parallel Multi-level Analytical Global Placement on Graphics Processing Units", in Proc. ICCAD, pages 681-688, San Jose CA, Nov 2009**
- J. Cong, W. Jiang, B. Liu, and Y. Zou, "Automatic Memory Partitioning and Scheduling for Throughput and Power Optimization", in Proc. ICCAD, , pages. 697-704, San Jose, CA, Nov 2009.
- J. Cong, K. Gururaj, W. Jiang, B. Liu, K. Minkovich, B. Yuan and Y. Zou, "Accelerating Monte-Carlo based SSTA using FPGA", in Proc. FPGA, pages 111-114, Monterey, CA, Feb 2010.
- **J. Cong and Y. Zou, "A Comparative Study on the Architecture Templates for Dynamic Nested Loops", in Proc. FCCM, pages 251-254, Charlotte, NC, May 2010**
- J. Cong, M. A. Ghodrati, M. Gill, C. Liu, G. Reinman and Y. Zou, "AXR-CMP: Architecture Support in Accelerator-Rich CMPs", in Proc.SAW-2, San Antonio, TX, Feb 2011.
- J. Cong, H. Huang, C. Liu and Y. Zou, "A Reuse-Aware Prefetching Algorithm for Scratchpad Memory", Proc. DAC, San Diego, CA, Jun 2011.
- **J. Cong, M. Huang and Y. Zou, "3D Recursive Gaussian IIR on GPU and FPGAs", Proc. SASP, San Diego, CA, Jun 2011.**
- J. Cong, K. Gururaj, H. Huang, C. Liu, G. Reinman and Yi Zou, "An Energy-Efficient Adaptive Hybrid Cache", Proc. ISLPED, Fukuoka, Japan, Aug 2011.
- **J.Cong, M. Huang and Y. Zou, "Accelerating Fluid Registration Algorithm on Multi-FPGA Platforms", Proc.FPL, Chania, Crete, Greece, Sep 2011**
- J. Cong, K. Gururaj, M. Huang, S. Li, B. Xiao and Y. Zou, "Domain-Specific Processor with 3D Integration for Medical Image Processing", Proc. ASAP, Santa Monica, CA, pp. 247-250, September 2011.
- J.Cong, P. Zhang and Y.Zou, "Combined Loop Transformation and Hierarchy Allocation for Data Reuse Optimization", Proc. ICCAD, , San Jose CA, Nov 2011
- **A. Bui, K.Cheng, J. Cong, L. Vese, Y. Wang, B. Yuan and Y. Zou, "Platform Characterization for Domain-Specific Computing (invited paper) ", Proc. ASPDAC, Sydney, Australia, Jan 2012**
- **J. Chen, J. Cong, M.Yan and Y. Zou, " FPGA-Accelerated 3D Iterative Reconstruction", Proc. FPGA, Monterey CA, Feb 2012**

Technical Reports

- M. Moazeni, Y. Zou, M. Rofouei, A. Bui, M. Sarrafzadeh and J. Cong, “A Performance Evaluation of General Purpose Applications on Multithreaded GPUs”, UCLA Technical Report 090003

Selected publications before I came to UCLA see <http://cadlab.cs.ucla.edu/~zouyi/Selected%20Publications.htm>