IPEM - Interconnect Performance Estimation Model

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http://cadlab.cs.ucla.edu/software_release/ipem/htdocs/

Interconnect Layout Optimization

- UCLA Tree-Repeater-Interconnect Opt. (TRIO) Package [Cong et al, ICCAD’97] as an example
  - Interconnect topology optimization
  - Optimal buffer insertion
  - Wiresizing optimization
  - Global interconnect sizing and spacing
  - Simultaneous driver, buffer, and interconnect sizing
  - ……
- Delay can be improved significantly (e.g., 5-10x)!
- Should be considered as early as possible for design convergence. ➔ IPEM
IPEM Problem Formulation

\[ R_{d0} \quad \text{driver effective resistance of the input stage} \ G_0 \]
\[ R_d \quad \text{driver effective resistance of} \ G \]
\[ l \quad \text{interconnect wire length} \]
\[ C_L \quad \text{loading capacitance} \]

What is the optimized delay/area, …?
(without running TRIO or other opt. tools!)

IPEM: Capabilities and Features

- **Capabilities (APIs):**
  - OWS (Optimal Wire Sizing)
  - SDWS (Simultaneous Driver and Wire Sizing)
  - BIWS (Buffer Insertion and Wire Sizing)
  - BISWS (Buffer Insertion, Sizing and Wire Sizing)
  - Calculate the critical length for buffer insertion with consideration of wire-sizing optimization
  - Default and user-specified technology parameters.

- **Features:**
  - simple closed-form formulae or computational procedures
  - constant running time in practice (10,000x faster than TRIO)
  - high accuracy (about 90% accuracy on average)
  - IPEM library easily linked to any program/tool
Parameters Used in IPEM

- length : length of interconnect, in \( \mu m \).
- Rd : driver resistance, in \( \Omega \).
- Cl : loading capacitance, in \( fF \).
- Rb : buffer resistance, in \( \Omega \).
- Cb : buffer capacitance, in \( fF \).
- tg : intrinsic device delay, in ps.
- \( k_{\text{max}} \) : the max \( k \). Driver’s size is supposed to be \( k \times (\text{min gate}) \).
- Rd0 : Effective resistance of the initial driver \( G_0 \), in \( \Omega \).
- Rb_array : buffer resistance array, each in \( \Omega \).
- Cb_array : buffer capacitance array, each in \( fF \).
- tg_array : buffer intrinsic delay array, each in ps.
- buf_n : number of available buffers available.
- layer_n : layer number.
- gen_n : technology generation number.

Example of IPEM under OWS

- **Closed-form** delay estimation formula

\[
T_{\text{ows}}(R_d, l, C_l) = \left[ \frac{\alpha_1 l}{W^2(\alpha \cdot l)} + \frac{2\alpha_1 l}{W(\alpha \cdot l)} + R_d C_f + \sqrt{R_d R_c C_f C_L} \right] \cdot l
\]

where

\[
\alpha_1 = \frac{1}{4} R C_a \quad \alpha_2 = \frac{1}{2} \sqrt{\frac{R C_a}{R_d C_L}}
\]

\( W(x) \) is Lambert’s \( W \) function defined as \( W e^W = x \)

- **Closed-form** area estimation formula

\[
A_{\text{ows}}(R_d, l, C_L) = \sqrt{\frac{r(c_f l + 2 C_l)}{2R_d C_a}} \cdot l
\]
IPEM vs. TRIO Using OWS

- 0.18um, $R_d = \frac{r_g}{100}$, $C_L = c_g \times 100$
- For expt., max wire width is 20x min, wire is segmented in every 10um

API Example for IPEM

```c
double Tows (length, Rd, Cl, layer_n, gen_n)
double length, Rd, Cl;
int layer_n, gen_n;
    # Estimate the interconnect delay, under optimal wire sizing.
    # Return the delay in ps (10^-12 seconds).
```

Critical Length for Buffer Insertion w/ OWS

- Solving critical length $l_{crit}(b, R_d, C_L)$
  - Computed by bisection method
  - Constant time in practice

$$L_{crit}(R_d, C_l, R_b, C_b, t_g, \text{layer}_n, \text{gen}_n)$$

double $R_d, C_l, R_b, C_b, t_g$
int $\text{gen}_n, \text{layer}_n$;

- Estimate critical length for buffer insertion under optimal wire sizing.
- Return the critical length, in um.

BIWS & BISWS

- BIWS (Simultaneous Buffer Insertion and Wire Sizing)
  - Insert buffer
  - Optimize wire size
- BISWS (Simultaneous Buffer Insertion, Sizing and Wire Sizing)
  - Insert buffer
  - Optimize buffer size
  - Optimize wire size
IPEM vs. TRIO Using BIWS

- $0.18 \text{ um}, R_d = r_g / 10$, $C_L = c_g \times 10$, buffer type is 100 x min.
- For expt., max. wire width is 20x min. width, wire is segmented in every 100um.

Application of IPEM

- Layout-driven RTL and physical level floorplanning.
- Considering interconnect opt. in logic level synthesis.
  - Use IPEM to predict accurate interconnect delay without really going into layout details
  - Use accurate interconnect delay to guide synthesis
- Interconnect Planning.
- MARCO/GSRC: GTX (Ground Truths/Technology Extrapolation).
- ....