Power Model for Interconnect Planning

Chin-Chih Chang‡, Jason Cong‡, Taku Uchino†, and Xin Yuan‡

† Toshiba Corporation, 580-1 Horikawa-cho, Saiwai-ku, Kawasaki 212-8520, Japan
‡ Computer Science Department, University of California, Los Angeles, CA 90095, U.S.A.

Abstract— This paper presents a power model for global interconnects. The power is divided into two parts, capacitive power and buffer power. The capacitive power for a net is estimated based on the tile structure, which represents the physical hierarchy for the interconnect planning. The buffer power is estimated based on the fact that the total short-circuit power is not sensitive to the buffer location. Experimental results show that our capacitance model is accurate even for a coarse tile structure. We have also studied the correlation between power consumption and total wire length at the interconnect planning stage using this power model.

I. Introduction

In deep sub-micron designs, interconnects dominate the performance of the LSI chip. As a result, the interconnect-centric design [1] is required. In the interconnect-centric design, the conventional design paradigm, which is based on the logical hierarchy is replaced by the new design paradigm based on the physical hierarchy as shown in Fig.1.

The physical hierarchy is represented as a series of the tile structures, each of which represents a level of the physical hierarchy. At each level of the physical hierarchy, the location of a cell is specified by the tile containing it, and the topology of a net is specified by a set of tiles that contains the routing path of the net (*cf.* Fig.2(a)). The finer the tile structure becomes, the more accurate the cell location and net topology become. The process of generating a sequence of rough placement and routing is called the *interconnect planning process* in the interconnect-centric design flow. In the interconnect planning process, area, delay, and power must be estimated for an optimal final layout result.

This paper proposes an interconnect power model for each level of the physical hierarchy. Since the model may be used repeatedly in the interconnect planning process, it should be simple as well as accurate. The most important feature of our model is that it can accurately estimate the coupling capacitance as it takes a large portion of the total wire capacitance in the deep sub-micron design. Our model also considers the power due to buffers as buffer insertion is a technique commonly used to reduce the interconnect delay.

The paper is organized as follows. Section II presents our interconnect power estimation model for the interconnect planning process. Section III discusses the application of our power model at the interconnect planning level. Section IV provides experimental results, and Section V concludes the paper.

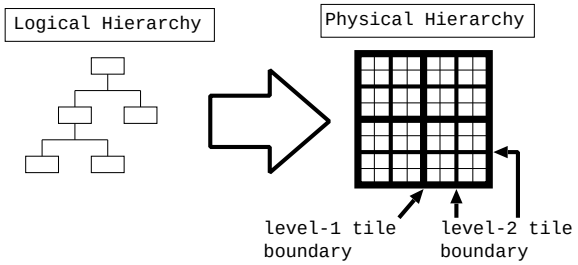

Fig. 1. Paradigm shift from the logical hierarchy to the physical hierarchy. In the logical hierarchy, the chip is composed of a set of logical modules which is denoted by boxes in the figure. On the other hand, the chip is divided into a set of tiles at each level of the physical hierarchy. The level of a fine tile structure is lower than that of a coarse one. In the figure, 2×2 tile structure is the top level, 4×4 tile structure is the next level, and so on.

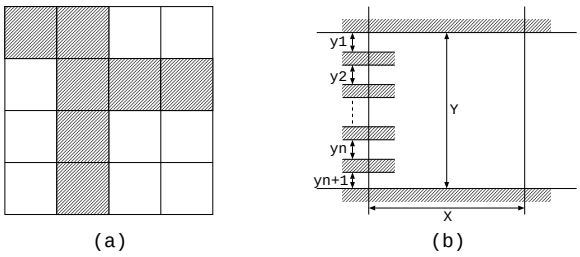

Fig. 2. (a) Each layer is divided into tiles. The rough location of a cell is represented by a tile which contains the cell. The rough topology of a net is represented by a set of tiles (shown in shaded areas) which contain the net. (b) Distribution of wires crossing a boundary of a tile. A shaded box represents an effective wire with effective width $w + s_{min}$. The shaded boxes on the top and bottom boundaries are wires in the adjacent tiles.

II. Our Power Estimation Model

In this section, we present our interconnect power model, and show how to calculate the model parameters based on the rough layout data, which is illustrated in Fig.2(a).

Let P_i denote the power consumption of net i. P_i is divided into the following two parts:

$$P_i = P_i^C + P_i^B, \tag{1}$$

where P_i^C denotes the power due to charging and discharging

of the load capacitance of net i, and P_i^B denotes the power due to the buffers to be inserted into net i. P_i^C and P_i^B are called *capacitive power* and *buffer power*, respectively, for net i. They are expressed as follows:

$$P_i^C = \frac{1}{2} f_i C_i V_{DD}^2, \tag{2}$$

and

$$P_i^B = \sum_{b=1}^{N_i} f_i E_b, \tag{3}$$

where f_i is the switching frequency[1] of net i, C_i is the load capacitance of net i, V_{DD} is the supply voltage, b represents the label of a buffer, N_i is the number of buffers to be inserted into net i (*cf.* Appendix B), and E_b is the internal energy of buffer b. E_b is the energy caused by a signal transition, and is considered as the sum of the energy due to the short-circuit current, and that of charging and discharging of the internal capacitance.

The inputs and outputs of our power estimator are summarized in Fig.3.

The switching frequency information f_i for each net i can be estimated prior to the interconnect planning process using any commercially available simulator, such as `Verilog-XL`.

The capacitance look-up table provides the unit-length area, fringe, and coupling wire capacitances under various wire widths and spacings. The capacitance look-up table is obtained using the 2-D extractor provided by the authors of [2].

The buffer look-up table provides the buffer internal energy consumption per transition for various input slew time and load capacitance. The buffer look-up table is obtained using `HSPICE`.

These look-up tables are used extensively in our power estimation process and will be shown in the following subsections.

A. Estimation of Capacitive Power

The load capacitance of net i, denoted by C_i in (2), is defined by

$$C_i = \sum_p C_p^P + N_i C_g + C_i^G + \sum_{j \neq i} \langle S_{ij} \rangle C_{ij}^X, \tag{4}$$

where p is the label for the input pins connected to net i, C_p^P is the input capacitance for pin p, N_i is the number of buffers, C_g is the input capacitance of a buffer, C_i^G is the ground wire capacitance[2], C_{ij}^X is the coupling capacitance between nets i and j, S_{ij} is the switching factor, and $\langle S_{ij} \rangle$ is its average. According to Appendix A, we can assume $\langle S_{ij} \rangle = 1$. In this paper, we shall show a method to estimate C_i^G and $\sum_{j \neq i} C_{ij}^X$. Other parameters can be easily obtained.

It is well known that the coupling and fringe capacitance strongly depends on the distance between adjacent parallel wires. Hence, the wire distance must be carefully considered in wire capacitance estimation.

[1]The switching frequency is the number of the signal transitions per unit time.

[2]The ground wire capacitance includes the area and fringe wire capacitance.

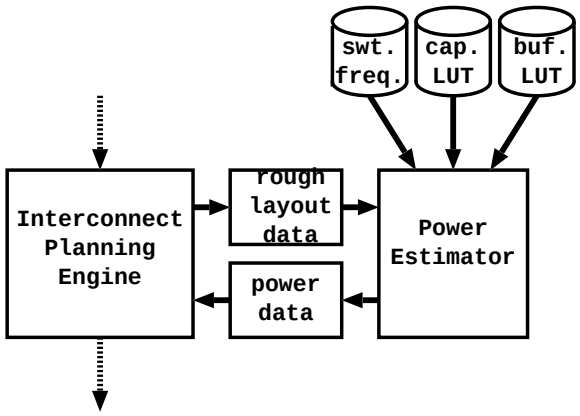

Fig. 3. Inputs and outputs of our power estimator, and the relation with the interconnect planning engine. "swt. freq." is the switching frequency information for each net, "cap. LUT" is the capacitance look-up table, and "buf. LUT" is the buffer look-up table. "power data" includes the estimated total power.

We assume that in addition to the rough location of the cells and nets, the following information is provided by the interconnect planning engine:

- X : the horizontal length of a tile,
- Y : the vertical length of a tile,
- w : the default wire width for each layer,
- s_{min} : the minimum spacing between wires,
- n : the number of the wires crossing each boundary.

Since the distance between adjacent parallel wires can not be less than s_{min}, it is convenient to consider each wire as having a width of $w + s_{min}$, which is called *effective width* in this paper. A virtual wire, whose width is broadened up to $w + s_{min}$, is called *effective wire*.

To estimate the wire distance, we have to consider the distribution of the wires within a tile. For simplicity, we concentrate on the horizontal wires crossing the left boundary of a specific tile on a specific layer as shown in Fig.2(b), in which the distribution of wires is represented by spacing parameters $y_1, \cdots, y_n$ where y_j ($j = 1, \cdots, n$) denotes the distance between the $(j-1)$-th effective wire and the j-th effective wire. We assume that effective wires exist in adjacent tiles on the top and bottom boundaries for later convenience.

Let $p(y_1, \cdots, y_n)$ denote the probability density of the distribution $y_1, \cdots, y_n$. Since the total probability is 1, the integration over all possible distributions must be 1:

$$\int_0^{Y'} dy_1 \int_0^{Y'-y_1} dy_2 \cdots \int_0^{Y'-y_1-\cdots-y_{n-1}} dy_n \quad p(y_1, \cdots, y_n) = 1, \tag{5}$$

where $Y' \equiv Y - n(w + s_{min})$.

The previous works, such as [4], assume that the average value of the coupling capacitance is represented by the value

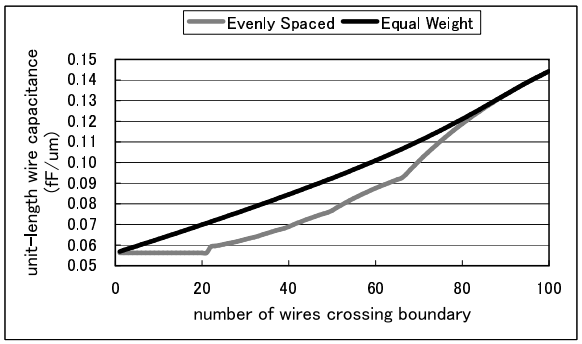

Fig. 4. Comparison of the unit-length capacitance estimation methods for $100nm$ technology. The capacitance obtained by "Evenly Spaced" method is estimated using a look-up table $c(y)$ with $y = Y'/(n+1)$ (wire distance for evenly spaced case). "Equal Weight" means our method based on the principle of equal weight. The horizontal axis represents the number of the wires crossing the boundary, where 100 is the maximum allowable number of the wires which can cross the boundary. The vertical axis represents the unit-length wire capacitance (ground + coupling) at the top layer.

when the wires are evenly distributed in a tile. This means $y_1 = y_2 = \cdots = y_n = Y'/(n+1)$ in Fig.2(b). However, this assumption is not realistic since the locations of the wires within a tile are not determined at the interconnect planning level, and there is no reason to assume the evenly spaced distribution. On the contrary, we would like to emphasize that *any* distribution of the wires can take place at equal probability. This means, for example, the distribution $y_1 = y_2 = \cdots = y_n = 0$ can take place at the same probability as the evenly spaced distribution. According to this *principle of equal weight*, $p(y_1, \cdots, y_n)$ is constant for any distribution $y_1, \cdots, y_n$, and is equal to $p = n!/\left(Y'\right)^n$ since the left hand side of (5) is $\left(Y'\right)^n/n!p$.

The probability distribution for y_1, which is denoted by $p(y_1)$, is obtained by integrating over all possible distributions for $y_2, \cdots, y_n$ as follows:

$$\begin{aligned} p(y_1) &= \int_0^{Y'-y_1} dy_2 \cdots \int_0^{Y'-\sum_{i=1}^{n-1} y_i} dy_n \; p \\ &= \frac{n}{Y'}\left(1 - \frac{y_1}{Y'}\right)^{n-1}. \end{aligned} \tag{6}$$

The probability distribution for $y_2, \cdots, y_n$ has the same form.

Using (6), the average unit-length capacitance at the boundary is obtained by

$$\bar{c} \equiv \int_0^{Y'} dy \; p(y)c(y) = \int_0^{Y'} dy \frac{n}{Y'}\left(1 - \frac{y}{Y'}\right)^{n-1} c(y), \tag{7}$$

where $c(y)$ denotes the unit-length capacitance as a function of the distance y between adjacent effective wires. This integral is performed numerically using $c(y)$ provided by the capacitance look-up table.

Fig.4 shows the difference between evenly spaced assumption and equal weight assumption. The difference is most obvious when the number of the wires crossing the boundary is about 20–70% of the capacity of the boundary.

Appendix C describes how to calculate C_i^G and $\sum_{j \neq i} C_{ij}^X$ based on the unit-length capacitance given by (7).

B. Estimation of Buffer Power

The internal energy of a buffer is due to:

1. charging/discharging of the internal capacitance,
2. static current,
3. short-circuit energy.

Of them, only the short-circuit energy can depend on buffer location since it is proportional to the input slew time, which is also proportional to the Elmore delay from the output of the previous buffer. Hence, the average short-circuit energy for a buffer in net i is proportional to

$$\frac{1}{N_i}\sum_{b=1}^{N_i} d_b, \tag{8}$$

where d_b is the Elmore delay from the output of the previous buffer to the input of buffer b. According to [3], the sum of the Elmore delays is not sensitive to the buffer locations. This also means

$$E_i^B \equiv \frac{1}{N_i}\sum_{b=1}^{N_i} E_b \tag{9}$$

is not sensitive to the buffer location as illustrated in Fig.5, where E_i^B is the average buffer internal energy per switching.

The above argument means we can assume any buffer location to estimate E_i^B. This observation is an important contribution of this paper. Since any buffer location is available to estimate E_i^B, we assume each buffer is located to drive the equal load capacitance $C \equiv C_i/N_i$, and to have the equal input slew time $s \equiv RC$, where

$$R \equiv \frac{1}{N_i}\sum_t r(t)L(t) \tag{10}$$

is the average load resistance for a buffer, and $r(t)$ is the unit-length resistance on tier[3] t. In this case, E_i is equal to $E(s, C)$, where $E(s, C)$ is the internal energy of a buffer for the input slew time s and load capacitance C. $E(s, C)$ is obtained from the buffer look-up table.

Using E_i^B, the buffer power is obtained by the following equation:

$$P_i^B = f_i N_i E_i^B. \tag{11}$$

III. Application of Our Model at Interconnect Planning

In a deep sub-micron interconnect centric design flow, it is important to design the global interconnects in the early design stages to guarantee performance and design closure. It is preferable for an interconnect planning engine to design and optimize the global interconnect since such an engine

[3]A tier is a pair of layers, on each of which either horizontal or vertical wires are routed.

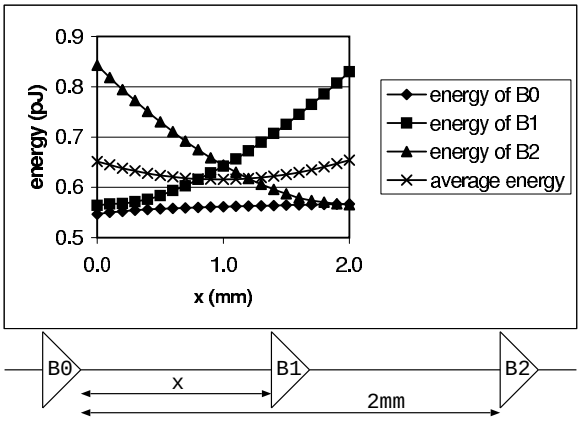

Fig. 5. Relation between energy and buffer location in $100nm$ technology obtained by HSPICE. "Average energy" is the average energy of three buffers, and is not sensitive to the location of $B1$.

(#row)×(#column)	average	maximum	total
2 × 2	52.7	154.9	-42.0
4 × 4	21.8	155.8	-5.0
8 × 8	12.9	96.4	2.3
16 × 16	6.5	86.7	2.8
32 × 32	3.8	36.0	2.2
64 × 64	2.1	18.4	1.1
128 × 128	1.1	11.1	0.3

TABLE I
LOAD CAPACITANCE ESTIMATION ERROR. THE FIRST COLUMN ((#ROW)×(#COLUMN)) INDICATES THE NUMBER OF THE ROWS AND COLUMNS OF THE TILE STRUCTURE. THE SECOND COLUMN (AVERAGE) SHOWS THE AVERAGE LOAD CAPACITANCE ESTIMATION ERROR (%) FOR EACH NET, WHERE THE AVERAGING IS DONE FOR THE ABSOLUTE VALUE OF THE ERROR. THE THIRD COLUMN (MAXIMUM) SHOWS THE MAXIMUM LOAD CAPACITANCE ESTIMATION ERROR (%) FOR EACH NET, WHERE THE ERROR IS THE ABSOLUTE VALUE. THE FORTH COLUMN (TOTAL) SHOWS THE TOTAL LOAD CAPACITANCE ESTIMATION ERROR (%).

can break down the logical hierarchy and generate a more reasonable physical hierarchy.

Since our power model only requires global placement and congestion information, it can be used in combination with an interconnect planning tool. It can be used in interconnect planning in two ways: (1) It can provide accurate power estimation for an interconnect planning solution so that any power problem in an interconnect planning solution can be discovered in the early design stages without going through any detailed placement and routing. (2) The interconnect planning tools can use the power estimation model to guide the optimization engine to generate planning with low power consumptions.

The advantage of using our power model for the power evaluation is quite clear as long as the model is accurate enough — it can provide a fast and accurate power estimation without taking a long time for detailed placement and routing. We shall show the accuracy of the model in the experimental result section to validate this claim.

The application of the power model to guide the interconnect planning may deserve some further discussion. It is well known that interconnect capacitance may have significant correlation with the total wire length. Therefore, before we use the power model to guide the interconnect planning tools directly, we should first find out how strong the correlation between total interconnect power and total wire length is. If the correlation between the total wire length and the total power is strong, we can simply use the total wire length to guide the interconnect planning engine and only apply the power model when exact and accurate power estimation is required to be calculated (for example, to ensure that the constraints in power consumption are satisfied). If the correlation is weak, we may need to tightly integrate the power estimation to the interconnect planning engine. In the next section, we have additional detailed data showing the correlation between the total power and the total wire length.

IV. EXPERIMENTAL RESULTS

A. Validation of Our Model

In this section, we will discuss the validation of the power estimation model. We used $180nm$ technology, in which $V_{DD} = 1.8V$. For simplicity, we assume $f_i = 0.12GHz$ for each net.

Table I shows the results of the experiment to confirm the accuracy of our load capacitance estimation. In this experiment, we use a test case *mcc1* which is obtained from [7]. According to [7], the mcc1 test case is generated by using the global routing in [6], pseudo pin assignment in [7] and detailed routing in [8]. It has 802 global interconnects and was scaled to $0.18\mu m$ technology.

To compare our model with this exact result, we divided the chip into an $n \times n$ tile structure, where $n = 2, 4, 8, 16, 32, 64, 128$, and counted the number of nets crossing each boundary. Based on this congestion information, we estimated the load capacitances of each net and compared it with the exact value computed based on the detailed routing solution.

According to Table I, our model is accurate even for a coarse tile structure such as 16 × 16 decomposition. The estimation error is mainly due to the following reasons. The detailed routing is not as simple as first estimated in our planning stage. The actual coupling capacitance for each net can not be accurately determined without knowing the actual wire length and wire spacing calculated from detailed routing, which may not be the same for different nets. Therefore, some estimation errors will be introduced in the coupling capacitance estimation in our model. Furthermore, some wires may also take detour routes within a tile. These detours can not be seen at the high level of physical hierarchy since we only know the congestion information at the tile boundaries. These detour routes will contribute more estimation errors to our model.

The error of the total load capacitance is smaller than the average or maximum one, and can be explained as follows:

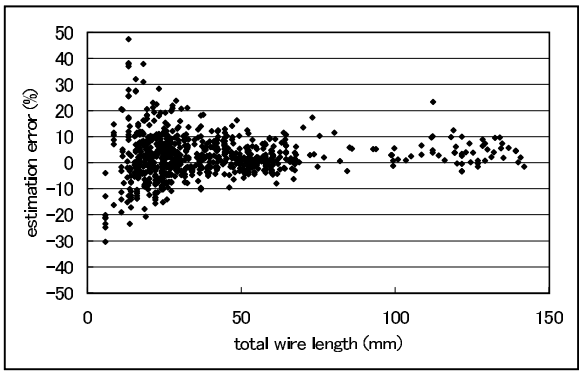

Fig. 6. Relation between load capacitance estimation error and wire length for 16 × 16 tile structure. The horizontal axis represents the total wire length of each net. The vertical axis represents the estimation error of the load capacitance. Each data point represents a net. A few data points are out of the range of this graph.

1. The estimation error of the load capacitance for each net can be minus as well as plus. Hence the error can be cancelled out each other when we sum up the load capacitance for each net to obtain the total load capacitance.

2. Our capacitance model is especially accurate for longer interconnects, which dominate the total load capacitance. This is because our probabilistic assumption works well since they cross many boundaries.

These observations are supported by Fig.6.

B. Correlation between Total Wire Length and Power

We use a set of MCNC standard cell benchmarks for the experiments on the correlation between total global interconnect wire length and total interconnect power consumption. The test cases are: s9234, s5378, s13207, s15850, s38417, s38584, bigkey and clma [4]. Table II shows the circuit's characteristics of these test cases.

We use the interconnect planning tool that is currently under development at UCLA [1] to generate an interconnect planning solution. Our interconnect planning tool places all the cells on the tiles and performs a global routing on it. We can restrict global routing to use only 1, 2, or 3 tiers, which result in different routing congestions.

Our interconnect planning tool uses simulated annealing based placement algorithm. Therefore, it is capable of generating multiple solutions for the same test case. For each test case, we generate multiple interconnect planning solutions with global routing restricted to different number of tiers. For each solution, we calculate the total bounding box wire length and estimate the power consumption using our model. For each circuit, we calculate normalized wire lengths by computing the average wire length and dividing all the wire lengths by this average length to get the normalized wire length. We do the same normalization for powers. We then calculate the normalized power to normalize wire length ratio for each test case. After the ratio for each run of each circuit is calculated, we will calculated the average ratio and standard deviation. The results for using only 1, 2 and 3 tiers of routing layers are shown in Table III, Table IV, and Table V, respectively.

From left to right in these tables, the columns show the test case name, the number of runs, the average total wire length, the average total power, the average maximum routing congestion, the deviation of maximum congestion , the average ratio of the normalized total power to the normalized total wire length, and the deviation of ratios. A plot of all the normalized total wire lengths vs. all the normalized total powers are also shown in Fig.7.

We can see that the results in Table III are the most congested and consumed the most power, while the results in Table V are the least congested and consumed the least amount of power. However, if we look at the average normalized power to wire length ratio, all the ratios are consistently close to 1 in all tables. It is also shown in Fig.7 that all the points are close to the line $y = x$.

This shows that the interconnect power has a very strong correlation to the total bounding box wire length. Therefore, using bounding box wire length should be good enough for guiding the minimization of interconnect power during the interconnect planning. It also suggests that the total power of any planning solution with total wire length TW can be estimated by $P_0 \times TW/TW_0$, where P_0 and TW_0 are the total power and the total wire length of the initial planning solution, respectively.

name	#GATE	#PI	#PO	#NET
s9234	1448	28	37	1476
s5378	1653	35	45	1688
s13207	3713	59	146	3772
s15850	4393	76	148	4469
s38417	11281	28	106	11309
s38584	14695	38	284	14733
bigkey	8831	228	197	9059
clma	30565	61	66	30626

TABLE II
BENCHMARK CIRCUITS CHARACTERISTICS.

V. CONCLUSIONS

In this paper, we presented a power model for global interconnects based on the tile structure of the physical hierarchy. In our model, the load capacitance of a net is estimated based

[4]The test cases that we obtained only contain net lists without cell library information. The cell geometry and pin locations used in placement are generated by using a Mississippi State University $0.8um$ Standard Cell Library. We then shrunk them to approximate the cells in the $0.18um$ technology. We also pruned out some nets and dangling gates in order to get an irredundant signal network. Therefore the numbers of gates and nets reported in Table II may be different from those other publications. We assume the clock frequency $F = 0.1GHz$. Because we do not have switching frequency for the nets, we randomly assign them to be between 0.1 to 0.3 of the clock frequency.

example	# of Runs	avg. Wire(mm)	avg. Power(mW)	avg. Max Cg	std. dev Max Cg	avg Ratio	std. dev Ratio
s9234	20	70.97	0.39	0.96	0.08	1.0001	0.0132
s5378	20	93.66	0.51	1.03	0.12	0.9997	0.0147
s15850	20	310.21	1.69	1.08	0.16	0.9998	0.0135
s13207	20	256.18	1.40	1.24	0.26	1.0001	0.0260
s38417	20	1241.03	9.81	1.36	0.12	1.0009	0.0574
s38584	24	3923.20	29.86	1.31	0.19	0.9976	0.0504
bigkey	20	424.25	3.81	1.06	0.28	1.0000	0.0402
clma	13	4564.47	58.98	1.28	0.21	0.9986	0.0354

TABLE III
CORRELATION BETWEEN TOTAL INTERCONNECT POWER AND TOTAL WIRE LENGTH (1 TIER ROUTING)

example	# of Runs	avg. Wire(mm)	avg. Power(mW)	avg. Max Cg	std. dev Max Cg	avg Ratio	std. dev Ratio
s9234	20	71.15	0.37	0.81	0.09	0.9998	0.0121
s5378	20	93.80	0.49	0.86	0.11	0.9998	0.0138
s15850	20	313.46	1.62	0.89	0.09	0.9999	0.0203
s13207	20	257.16	1.36	0.94	0.16	0.9999	0.0154
s38417	20	1224.48	8.63	0.96	0.11	0.9986	0.0430
s38584	24	3905.19	25.68	0.92	0.16	0.9992	0.0420
bigkey	20	427.55	3.16	0.83	0.13	0.9997	0.0382
clma	13	4560.03	48.13	0.85	0.10	0.9995	0.0356

TABLE IV
CORRELATION BETWEEN TOTAL INTERCONNECT POWER AND TOTAL WIRE LENGTH (2 TIERS ROUTING)

example	# of Runs	avg. Wire(mm)	avg. Power(mW)	avg. Max Cg	std. dev Max Cg	avg Ratio	std. dev Ratio
s9234	20	70.75	0.37	0.77	0.11	0.9998	0.0155
s5378	20	93.16	0.49	0.87	0.12	0.9998	0.0146
s15850	20	313.92	1.64	0.85	0.15	0.9998	0.0170
s13207	20	256.43	1.34	0.89	0.14	0.9999	0.0171
s38417	20	1204.66	8.29	0.83	0.10	1.0018	0.0636
s38584	24	3887.59	25.26	0.82	0.15	0.9982	0.0502
bigkey	20	427.66	3.00	0.74	0.10	0.9999	0.0218
clma	13	4576.86	49.12	0.69	0.09	1.0011	0.0508

TABLE V
CORRELATION BETWEEN TOTAL INTERCONNECT POWER AND TOTAL WIRE LENGTH (3 TIERS ROUTING)

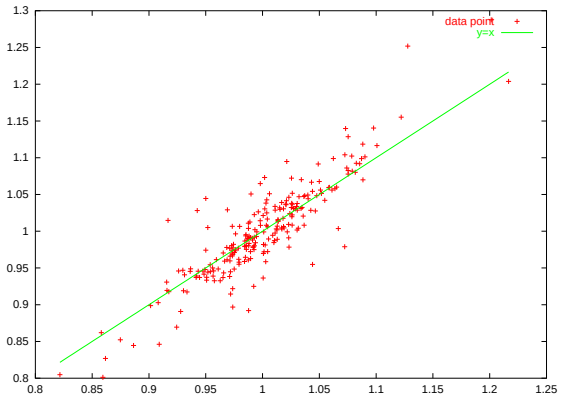

Fig. 7. Normalized power vs. normalized wire length plot

on the principle of equal weight for the wire distribution at the tile boundaries. The buffer power is estimated based on the fact that the average buffer power is not sensitive to the buffer location. We also studied the correlation between power consumption and total wire length at the interconnect planning stage using this power model.

Experimental results showed that our capacitance model is accurate enough even for a coarse tile structure.

APPENDIX

A. Estimation of Switching Factor

It is well known that $S_{ij} = 0$ if the signals on net i and j switch in the same direction, and $S_{ij} = 2$ if they switch in the opposite direction. When one of them is quiet, $S_{ij} = 1$. The number of the switchings in the same direction is almost equal to that of the switchings in the opposite direction when the signals on net i and j are mutually independent. In this case, $\langle S_{ij} \rangle = \frac{1}{2}(0+2) = 1$. The rigorous proof of this observation can be found in [9]. Since most of the signals are considered mutually independent in the real design, we can assume $\langle S_{ij} \rangle = 1$ in (4).

B. Estimation of the Number of Buffers

N_i is estimated using `IPEM` [5] as follows. We assume

$$N_i = \sum_t \frac{L(t)}{L_{crit}(t)}, \tag{12}$$

where $L(t)$ is the wire length of the net on tier t, and $L_{crit}(t)$ is the critical wire length for buffer insertion on tier t. $L_{crit}(t)$ is obtained using an API function of `IPEM`. To estimate $L(t)$, we can employ the same method as **STEP 2** and **STEP 3** in Appendix C by replacing both $\bar{c_1}$ and $\bar{c_2}$ with 1.

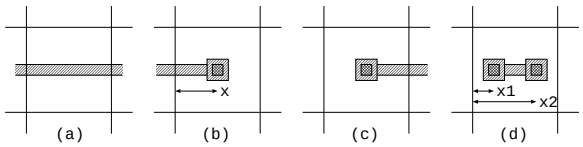

Fig. 8. (a) A wire goes through a tile. (b) A wire comes from the left and ends inside a tile. (c) A wire starts inside a tile and goes to the right. (d) A wire starts and ends inside a tile.

C. Estimation of Capacitance

In the following, C_* denotes either C_i^G or $\sum_{j \neq i} C_{ij}^X$, and the word "capacitance" represents either ground wire capacitance or coupling wire capacitance. The estimation of C_* is divided into the following three steps.

STEP 1: Estimation of unit-length capacitance,

STEP 2: Estimation of capacitance inside a tile,

STEP 3: Estimation of C_*.

STEP 1: Estimation of Unit-Length Capacitance The unit-length capacitance at each boundary is calculated by using (7).

STEP 2: Estimation of Capacitance inside a Tile

Using interpolation, the unit-length capacitance inside the tile is approximated as

$$\bar{c}(x) = \left(1 - \frac{x}{X}\right)\bar{c_1} + \frac{x}{X}\bar{c_2}, \tag{13}$$

where x is the distance from the left boundary, and $\bar{c_1}$ ($\bar{c_2}$) is the unit-length load capacitance at the left (right) boundary calculated by (7).

The capacitance of a wire segment inside the tile is calculated for each case shown in Fig.8.

Case (a): $C(0, X)$ denotes the capacitance of the wire segment. It is obtained by integrating $\bar{c}(x)$ along the wire segment as follows:

$$C(0, X) = \int_0^X dx \bar{c}(x) = \frac{X}{2}(\bar{c_1} + \bar{c_2}). \tag{14}$$

Case (b): $C(0, x)$ denotes the capacitance of the wire segment, where x is the location of the end point. By integrating $\bar{c}(x)$ along the wire segment, we obtain

$$C(0, x) = \int_0^x dx' \bar{c}(x'). \tag{15}$$

Since we do not have the information about the location of the end point, we assume x is uniformly distributed between 0 and X. In this case, the average capacitance, which is denoted by $C(0, *)$, is

$$C(0, *) = \frac{1}{X}\int_0^X dx C(0, x) = \frac{X}{6}(2\bar{c_1} + \bar{c_2}). \tag{16}$$

Case (c): Using the similar method to obtain (16), the average capacitance for the wire segment, which is denoted by $C(*, X)$, is

$$C(*, X) = \frac{X}{6}(\bar{c_1} + 2\bar{c_2}). \quad (17)$$

Case (d): $C(x_1, x_2)$ denotes the capacitance of the wire segment, where x_1 and x_2 are the locations of the end points. By integrating $\bar{c}(x)$ along the wire segment, we obtain

$$C(x_1, x_2) = \int_{x_1}^{x_2} dx' \bar{c}(x'). \quad (18)$$

Since we do not have the information about the location of the end points, we assume x_1 and x_2 are uniformly distributed between 0 and X with the condition $x_1 < x_2$. In this case, the average capacitance, which is denoted by $C(*, *)$, is

$$\begin{aligned} C(*,*) &= \frac{2}{X^2}\int_0^X dx_1 \int_{x_1}^X dx_2 C(x_1, x_2) \\ &= \frac{X}{6}(\bar{c_1} + \bar{c_2}). \end{aligned} \quad (19)$$

STEP 3: Estimation of C_*

C_* is the sum of the capacitances for the wire segments contained in the tiles, which determine the rough topology of the net. This means

$$C_* = \sum_{a \in T_i} C_i(a), \quad (20)$$

where T_i is the set of the tiles which represent the rough topology of the net, and $C_i(a)$ is the sum of the capacitances for the horizontal and vertical wire segments in tile a.

To calculate $C_i(a)$, we apply case (a), (b), and (c) of **STEP 2** according to the rough topology of the net. For example, if the left and right boundaries of tile a are shared by the other tiles in T_i, case (a) is applied. Also, if the left and bottom boundaries of tile a are shared by the other tiles in T_i, case (b) and its vertical correspondence are applied.

When the net has pins inside tile a, the wires connecting the pins to the net, must be also considered. Since these wires are completely contained in tile a, case (d) of **STEP 2** can be applied. We assume the total capacitance for these wires is the sum of the capacitance obtained by (19) and its vertical correspondence. This capacitance is also included into $C_i(a)$.

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