TIMING CLOSURE FOR ULTRA DEEP SUBMICRON DESIGN

ASP-DAC 2001, Yokohama
Tutorial 3

Presenters:

Jason Cong - University of California, Los Angeles
Olivier Coudert - Monterey Design Systems
Patrick Groeneveld - Magma Design Automation
Lou Scheffer – Cadence Design Systems

Tutorial Outline

- Part I: Introduction (Jason Cong)
- Part II: Timing closure today (Lou Scheffer)
- Part III: Gain-based synthesis (Patrick Groeneveld)
- Part IV: Physical design closure (Olivier Coudert)
- Part V: New approaches to harness global interconnects (Jason Cong)

Tutorial Schedule

- 09:30am: Introduction (Jason Cong)
- 09:40am: Timing closure today (Lou Scheffer)
- 10:50am Break
- 11:10am: Gain-based synthesis (Patrick Groeneveld)
- 12:30pm: Lunch
- 02:00pm: The Quest for design closure (Olivier Coudert)
- 03:20pm: Coffee Break
- 03:40pm: New approaches to harness global interconnects (Jason Cong)
- 05:00pm: Wrap-up and conclusions

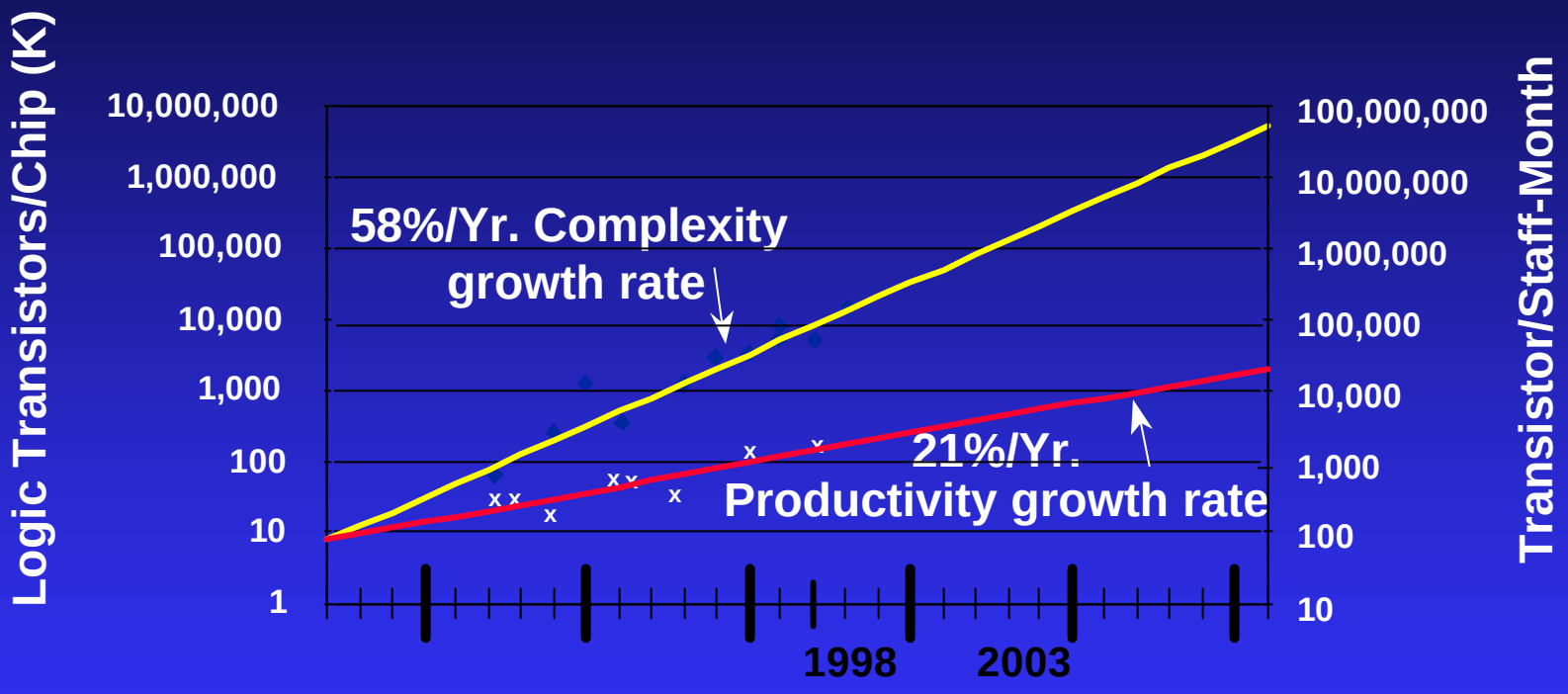
Exponential Growth of Chip Capacity

- **Moore's Law**
  - **Min. transistor feature size decreases by 0.7X every three years**
  - **True for at least 30 years! (first published in April 1965)**
- **1997 National Technology Roadmap for Semiconductors**

Technology (um)	*0.25*	*0.18*	*0.15*	*0.13*	*0.10*	*0.07*
Year	1997	1999	2001	2003	2006	2009
# transistors	11M	21M	40M	76M	200M	520M
On-Chip Clock (MHz)	750	1200	1400	1600	2000	2500
Area (mm^2)	300	340	385	430	520	620
Wiring Levels	6	6-7	7	7	7-8	8-9

- **Enables system-on-a-chip integration**

Productivity Gap
- Where Moore Law May Break



Chip Capacity and Designer Productivity

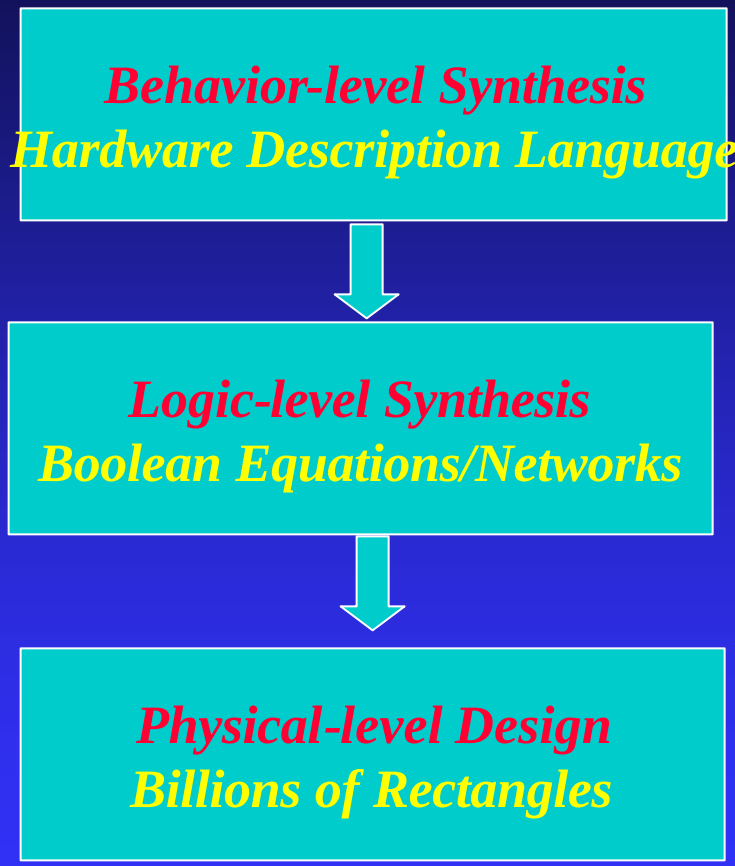
Source: NTRS'97

Approaches to Increase Design Productivity

- Raise level of design abstraction
- Use hierarchical design

Both require synthesis and layout timing closure

Levels of Abstraction in VLSI Design



Difficulties in Maintaining High-Level Abstraction & Hierarchical Design

- Interconnect delay far dominates device delay
  - Can no longer design in behavior/functional domain

Technology (um)	*0.25*	*0.18*	*0.15*	*0.13*	*0.10*	*0.07*
Intrinsic gate delay (ns)	0.071	0.051	0.049	0.045	0.039	0.022
1mm (ns)	0.059	0.049	0.051	0.044	0.052	0.042
2cm no-opt (ns)	2.589	2.48	2.65	2.62	3.73	4.67
2cm best-opt (ns)	0.895	0.793	0.77	0.7	0.77	0.672

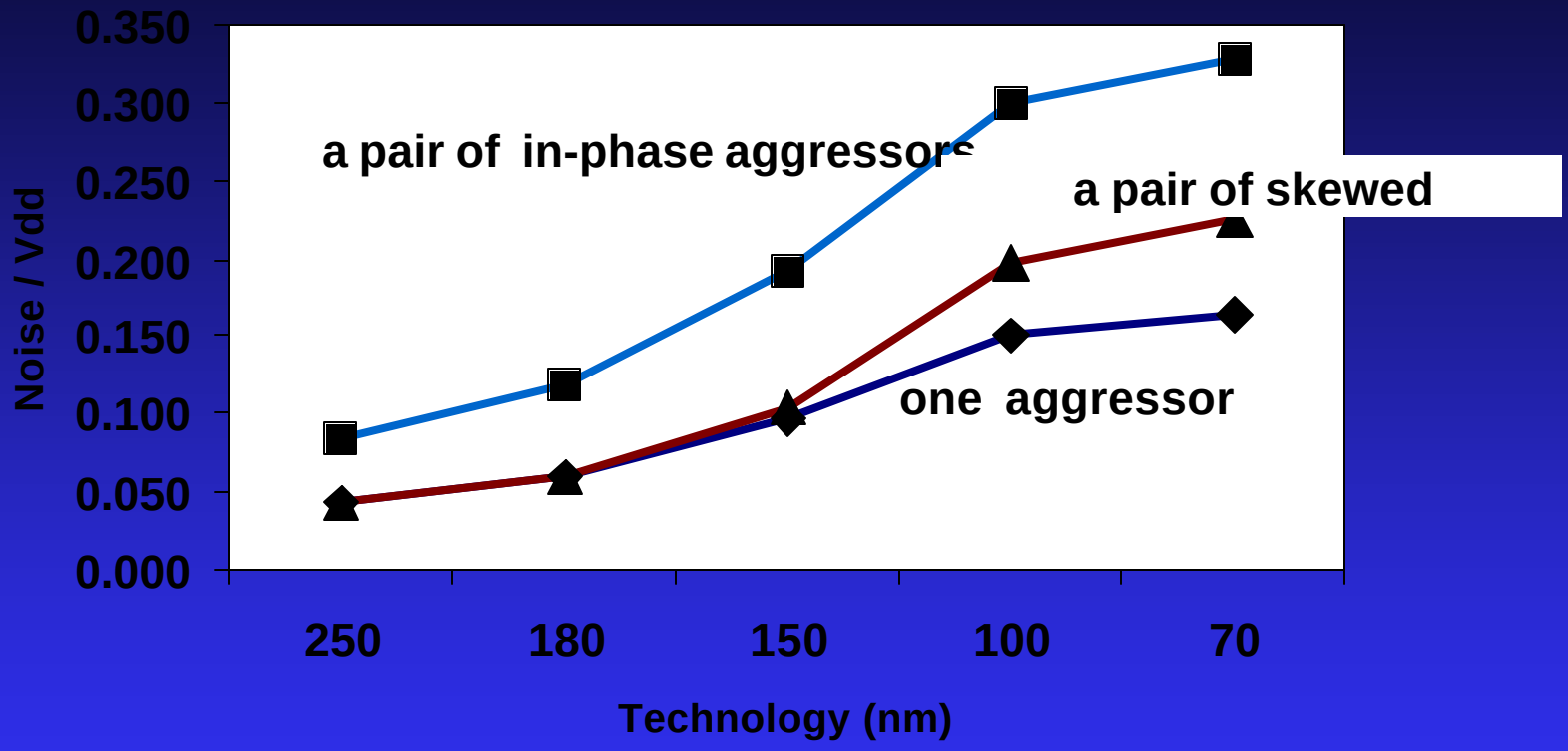
- Best-opt uses simultaneous buffer insertion, driver/buffer sizing, and wiresizing
- Reverse scaling of higher metal layers were not considered
- Source: [Cong97] SRC Working Papers http://www.src.org/research/frontier.dgw

Difficulties in Maintaining High-Level Abstraction & Hierarchical Design

- Current design hierarchy is based on functionality
  - interconnect delay
  - crosstalk
  - P/G bounce due to simultaneous switching, etc …

  => do not fit naturally into function hierarchy

Coupling Noise Problem



Coupling noise from two adjacent aggressors to the middle victim wire (1 mm) with 2x min. spacing. Rise time is 10% of projected clock period.

- **Coupling noise depends strongly on both spatial and temporal relations!**

Tutorial Outline

- Part I: Introduction (Jason Cong)
- Part II: Timing closure today (Lou Scheffer)
- Part III: Gain-based synthesis (Patrick Groeneveld)
- Part IV: Physical design closure (Olivier Coudert)
- Part V: New approaches to harness global interconnects (Jason Cong)